

Different Behaviour of Frequency Stability Measures in Independent and Synchronized Clocks: Theoretical Analysis and Measurement Results

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Abstract

The problem of characterizing synchronization performance plays a central role in the design of SDH based telecommunication networks. Moreover, establishing the suitable quantities for characterizing frequency stability of timing signals, together with their measurement configurations, is still an open issue in Standardization Committees. In this paper, we deal with some of the most important frequency stability quantities. An analysis envisaging the possibility to theoretically assess such quantities is carried out showing that substantial differences are expected in the behaviour of the above mentioned quantities, depending on the measurement configuration adopted. Besides, a high precision measurement set-up was used to derive experimental results which confirm the main theoretical conclusions and, at the same time, provide good insight into the behaviour of various stability measures.

1. Introduction

As the introduction of transmission systems based on SDH (Synchronous Digital Hierarchy) in the public networks is drawing near, the need for adequate synchronization facilities becomes more and more stringent in order to fully exploit the new capabilities of such synchronous systems. The design and the assessment of a synchronization network, based on a widespread deployment of synchronization units (clocks), both within *ad hoc* node synchronizing equipment and within SDH equipment, requires standard criteria and test configurations for the evaluation of frequency and time stability.

During the last few years, an intense debate on the choice of best parameters and methods for the assessment of synchronization performance has been going on within the regulatory organisms, mainly focusing on the following issues concerning the different stability quantities: their capability of recognizing the type of noise affecting timing signals, their theoretical and practical "soundness", their sensitivity to deterministic frequency offset and drift, their helpfulness in designing synchronizer and desynchronizer buffers required in synchronous equipment. Previous discussion in telecommunication standardization committees has neglected to explicitly define measurement configurations set-ups, though it is expected that different test configurations may strongly impact on the behaviour of measured quantities and on their general trends, as will be shown later on.

In this paper, we discuss the different behaviours of some of the most important time domain quantities, defined in the literature in

order to characterize frequency and time stability of oscillators, considering both the independent and the synchronized clock configurations, and comparing, when available, their trends evaluated either through the equations of a theoretical model or starting from real measurement results.

In section 2, we present a general model of the timing signal generated by a clock, along with the main related functions based on which time domain quantities we deal with in this paper, viz. *Allan Variance* (AVAR), *Modified Allan Variance* (MAVAR), *Time Variance* (TVAR), and the *root mean square Time Interval Error* (TIE_{rms}), are defined. We also introduce the concept of measuring time error between independent clocks or between synchronized clocks.

In section 3, two different approaches for the evaluation of frequency and time stability are described, the first being derived from a theoretical model and the second being based on the use of a measurement set-up for the acquisition of time error data.

In section 4, some results on the mentioned stability measures are reported: in sect. 4.1 the theoretical approach is considered, summarizing the state of our studies and showing some interesting results stemming from the application of numerical integration methods for the calculation of the Allan variance; in sect. 4.2 experimental results obtained by using the aforementioned set up are presented, discussing more in detail the measurement conditions and reporting on the behaviour of all the four stability quantities considered.

2. Timing Signal Model and Frequency Stability Measures

In this section, starting from a general mathematical description of timing signals, some important definitions of parameters and quantities which model the behaviour of *clocks* - i.e., devices intended to supply synchronization and timing to telecommunications systems - are introduced, along with the main statistical quantities used for characterizing time and frequency stability.

2.1. Timing Signal Model and Related Quantities

A general expression describing a pseudo-periodic waveform which models the timing signal $s(t)$ at the output of clocks is given by [1,2]

$$s(t) = A \sin \Phi(t) \quad (1)$$

where A is a constant amplitude coefficient and $\Phi(t)$ is the *total instantaneous phase*.

A perfectly periodic timing signal implies a linearly increasing $\Phi(t)$ according to $\Phi(t)=2\pi v_{\text{nom}}t$, where v_{nom} is called *nominal frequency* of the clock. For actual clocks the *instantaneous frequency* concept applies, formally defined as $1/(2\pi)$ times the derivative of $\Phi(t)$ with respect to time t , and commonly denoted by $v(t)$. A common model used to characterize $v(t)$ in most clocks for telecommunications applications is given by

$$v(t) = v_{\text{nom}} + \Delta v + Dv_{\text{nom}}t + \frac{1}{2\pi}\dot{\phi}(t) \quad (2)$$

where Δv represents the *frequency offset* from the nominal value v_{nom} , D is the *linear fractional frequency drift* rate, mainly describing oscillator ageing effects, and $\dot{\phi}(t)/(2\pi)$ is a *random frequency deviation* modelling oscillator intrinsic phase noise sources. Integrating $v(t)$ the total instantaneous phase is obtained

$$\Phi(t) = 2\pi(v_{\text{nom}} + \Delta v)t + \pi Dv_{\text{nom}}t^2 + \phi(t) + \Phi_0 \quad (3)$$

where $\phi(t)$ is the *random phase deviation* and Φ_0 is a constant phase delay. Two functions strictly related to $\phi(t)$ and $\dot{\phi}(t)$ are used in treating random frequency and time fluctuations: the *random fractional frequency deviation* $y(t)$ and the *random time deviation* $x(t)$, defined as

$$y(t) = \frac{\dot{\phi}(t)}{2\pi v_{\text{nom}}} \quad , \quad x(t) = \frac{\phi(t)}{2\pi v_{\text{nom}}} \quad (4)$$

The above models and definitions have been widely used by specialists in the field of oscillator stability characterization and measurement. More recently, the particular needs risen in the telecommunications world for the design of synchronization equipment and networks led to the introduction of some functions more oriented to the timing aspects of clocks. Here below we report the definition of the most important of such functions which will be useful in the subsequent discussion.

The *Time function* $T(t)$ of a clock is defined, in terms of its total instantaneous phase, as

$$T(t) = \frac{\Phi(t)}{2\pi v_{\text{nom}}} \quad (5)$$

It is worthwhile noticing that for an ideal clock $T_{\text{id}}(t)=t$ holds, as expected.

For a given clock the *Time Error function* $\text{TE}(t)$ between its time $T(t)$ and a reference time $T_{\text{ref}}(t)$, is defined as

$$\text{TE}(t) = T(t) - T_{\text{ref}}(t) \quad (6)$$

Finally, the time error variation over an interval duration τ is called *Time Interval Error* $\text{TIE}(t;\tau)$ and is defined as

$$\text{TIE}(t;\tau) = \text{TE}(t+\tau) - \text{TE}(t) \quad (7)$$

2.2. Quantities for Characterizing Frequency and Time Stability

We note that $\phi(t)$, $x(t)$ and $y(t)$ are random processes which are commonly characterized in terms of their Power Spectral Densities (PSD). Main results [3] deriving from theoretical analysis and experimental measurements show that most free running oscillators are typically affected by internal phase noise obeying the so-called *power law model*. In terms of $S_y(f)$, i.e. the PSD of $y(t)$, such model is expressed by

$$S_y(f) = \begin{cases} \sum_{\alpha=n_1}^{n_2} h_{\alpha} f^{\alpha} & 0 \leq f \leq f_h \\ 0 & f > f_h \end{cases} \quad (8)$$

where f_h is an upper cut-off frequency. The most common components found in typical oscillators are white Phase Modulation (PM) for $\alpha=2$, flicker PM for $\alpha=1$, white Frequency Modulation (FM) for $\alpha=0$, flicker FM for $\alpha=-1$, and random walk FM for $\alpha=-2$.

While the above frequency domain characterization proves to be very meaningful and complete, it requires sophisticated measurement equipment and methodologies: mainly for this reason time domain techniques, based on the use of digital counters, have been developed which extract a sampled version of the function $\text{TE}(t)$.

Starting from this sequence, various quantities, defined to characterize frequency and time stability, can be estimated: in our discussion we will consider the Allan variance $\sigma_y^2(\tau)$, the modified

Allan variance $\text{mod } \sigma_y^2(\tau)$, the time variance $\sigma_x^2(\tau)$ and the root mean square time interval error $\text{TIE}_{\text{rms}}(\tau)$. As far as the formal definitions of these quantities and the corresponding estimator formulas are concerned, the reader is referred to papers [4,5].

2.3. Impact of Measurement Configuration

Referring to the time domain approach, the problem of choosing the most appropriate measurement configuration for extracting TE data at the output of the Clock Under Test (CUT) arises.

Aiming at the estimation of ideal TE, i.e. the time error with respect to ideal time t , the actual Measurement Reference Clock (MRC) must perform, as a minimum, like a Primary Reference Clock (PRC) [6], so that the effects of its instabilities are negligible with respect to those of the CUT. This situation, which will be referred to as *independent clock* configuration, is depicted in fig. 1a.

When considering slave clocks two different operation modes exist, namely *free running mode* and *locked mode*. While for the first mode the independent clock configuration applies, for the second one an alternative configuration can be set-up, as shown in fig. 1b where the master clock synchronizing the CUT coincides with the MRC: this configuration is referred to as *synchronized clock* configuration.

Both the independent and synchronized configuration measurements provide useful information on clock performance [7] and are widely used in the laboratory and in the field. Unfortunately, as will be shown in the following, the two configurations lead to different behaviour in the stability quantities calculated from the TE data.

3. Evaluation of Frequency Stability Quantities

Two different approaches for the evaluation of frequency and time stability are described in this section. In sect. 3.1, from a theoretical model of slave clock, the procedure to analytically derive frequency domain expressions of stability measures is outlined. In sect. 3.2, an experimental approach based on the use of a measurement set-up for the acquisition of time error data is presented.

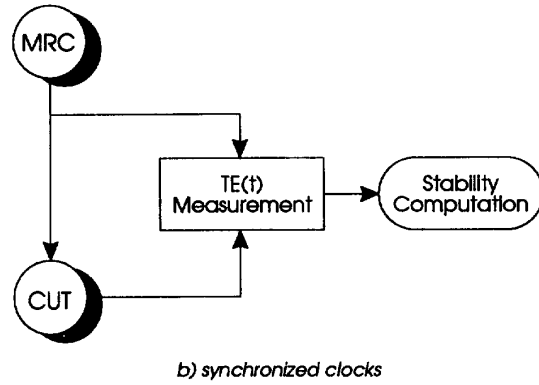
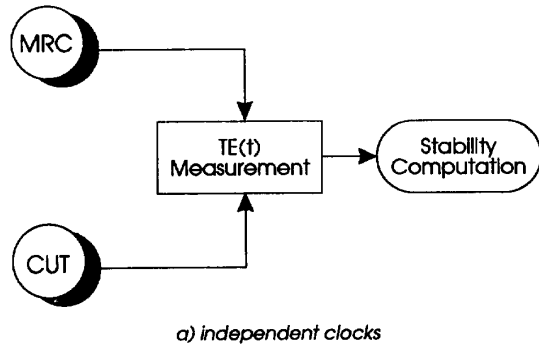


Fig. 1: Different configurations for clock stability measurements (MRC = Measurement Reference Clock, CUT = Clock Under Test)

3.1. Theoretical Approach

Based on the definition of the time domain stability quantities, and assuming the stationarity and ergodicity of $\varphi(t)$, integral relationships can be found between each quantity and

$$S_{\varphi}(f) = S_y(f) \left(\frac{v_{\text{nom}}}{f} \right)^2 \quad (9)$$

These relationships, which are reported in [4], can be used to theoretically evaluate the stability quantity behaviour due to the random component only in the phase model of eqn. (3), once that $S_{\varphi}(f)$ is known. As far as the free running oscillators are concerned, the power law model holds (see sect. 2.2); for the locked clock case a suitable modelling has been carried out starting from previous investigations [3,8].

The general model has been specialized in order to represent the essential operation of a slave clock (fig. 2). The meaning of symbols in fig. 2 is as follows: φ_r [rad] is the phase noise on the reference signal, φ_0 [rad] is the phase noise on the output of the locked slave clock, φ_{VCO} [rad] is the phase noise due to the Voltage Controlled Oscillator (VCO), K_d [V/rad] is the *Phase Detector* gain, K_0 [rad/(V·s)] is the VCO gain, $F(s)$ is the *Loop Filter* transfer function.

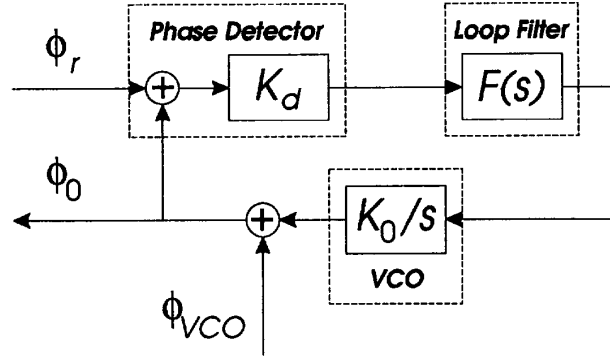


Fig. 2: Locked slave clock noise model

As anticipated in sect. 2.2 and according to [3,8], the PSD of internal noise φ_{VCO} for quartz crystal oscillators obeys the law

$$S_{\text{VCO}}(f) = \frac{c_3}{f^3} + \frac{c_2}{f^2} + \frac{c_1}{f} + c_0 \quad [\text{rad}^2 / \text{Hz}] \quad (10)$$

where c_0 , c_1 , c_2 , and c_3 are device dependent parameters. Note that in eqn. (10) the highest order term is the flicker FM component. Furthermore, for the device we considered in deriving the results of sect. 4.1, the coefficient c_2 referring to white FM component, had a very small value and then was neglected.

With a straightforward analysis the transfer function between noise injection point and slave clock output can be calculated

$$H(s) = \frac{s}{s + K_0 K_d F(s)} \quad (11)$$

and used to obtain phase noise PSD $S_{\varphi}(f)$ at the output

$$S_{\varphi}(f) = S_{\text{VCO}}(f) |H(j2\pi f)|^2 \quad [\text{rad}^2 / \text{Hz}] \quad (12)$$

3.2. Measurement Set-Up for Time Error Data Acquisition

To perform efficiently data acquisition and processing we conceived the high precision measurement set-up outlined in fig. 3. It is mainly based on a high performance time counter, with a resolution of 200 ps, comparing two timing signals $CK_{\text{Ref}}(t)$ and $CK_{\text{Test}}(t)$, and driven by a personal computer via a GPIB IEEE488.2 interface.

The time counter measures time intervals between two trigger events, e.g. two consecutive signal zero-crossings on input channels *A* and *B*, according to the time base at the *sync* input channel. A highly stable Rubidium frequency standard generates the timing signal $CK_{\text{Ref}}(t)$, which locks the device under test while operating in locked mode and, sent to the time counter channels *B* and *sync* inputs, works as common reference timing signal for the measurement.

Therefore, with this measurement configuration we are able to sample the process $TE(t)$ of the device under test relative to the reference time generated by the Rubidium frequency standard. Sequences of TE samples can be acquired by means of the personal computer, running a special purpose real-time software, and stored for any later numerical processing. Different sampling rates can be settled via the personal computer, while the upper limit of the total number of samples is bounded by the hard-disk storage capability.

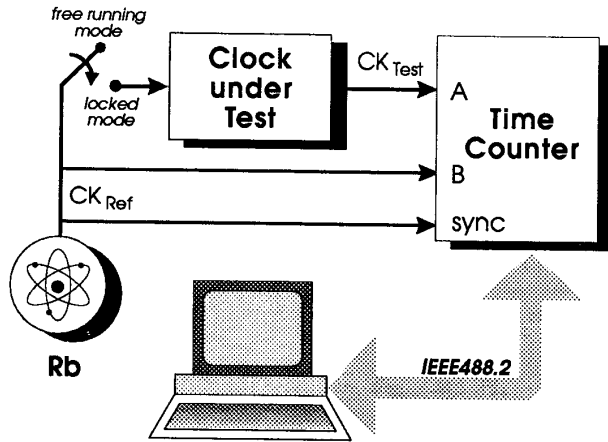


Fig. 3: $TE(f)$ measurement and data acquisition test-bed

4. Comparison of Theoretical and Measurement Results for Free Running and Slave Clocks

This section reports on some analytical and experimental results. In sect. 4.1, the state of our investigations concerning clock modelling and stability measure calculation is summarized, showing some interesting aspects resulting from the application of numerical integration methods for the calculation of Allan variance. In sect. 4.2, experimental results obtained by using the proposed measurement set-up are presented, discussing more in detail the measurement conditions and reporting on the behaviour of all the four stability quantities considered.

4.1. Theoretical Model Results

Referring to the integral relationships mentioned in sect. 3.1, our investigations concluded that closed form integration may result unfeasible even for the simplest cases; therefore a numerical approach must be adopted. The following considerations summarize the state of our studies, showing the present limitations of the theoretical approach.

□ TIE_{rms}

For the case of independent clock configuration, the integral expression of TIE_{rms} is theoretically not convergent if $S_{\phi}(f)$ has flicker or random walk FM components: this conclusion was confirmed running our numerical approximation software. No convergence issues arise for the synchronized clock configuration with the assumed phase noise model in eqn. (10): results on our investigations are reported in [8,9,10].

□ Allan variance

One of the most important features of this quantity is its analytical convergence, for both types of configurations in fig. 1 and for all noise types of interest. Our numerical routines allow to evaluate the Allan variance: results for a slave clock are reported in fig. 4 comparing free running and locked modes.

Observing this figure one can foresee that while Allan variance measurements in independent and synchronized configurations would give the same results in the short term (i.e., for observation intervals shorter than $1/B$), substantial differences would be found in the long term.

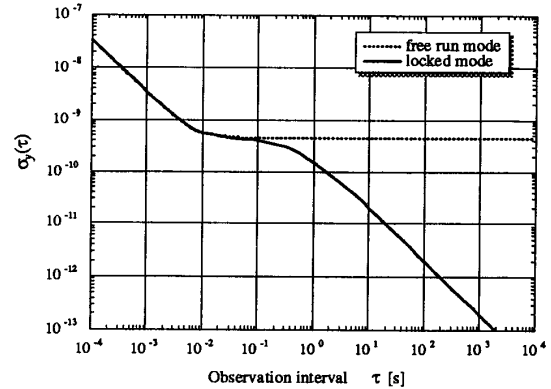


Fig. 4: Comparison of the Allan variance square root evaluated in free running and locked modes at the output of a slave clock operating at 5 MHz with loop bandwidth $B=1$ Hz

□ Modified Allan variance and time variance

Also for this two quantities, the same considerations on the analytical convergence discussed with reference to Allan variance apply: furthermore, it is well known that these two variances, strictly related each other, surpass the standard Allan variance in distinguishing between white and flicker PM. Unfortunately, the numerical integration of their frequency domain expressions proves very difficult: though a possible solution is currently under test, no definitive results are available yet.

4.2. Measurement Results

By means of the measurement set-up described in sect. 3.2, we studied the behaviour of a Synchronization Supply Unit (SSU) serving a telephone exchange and equipped with a Quartz oscillator, and with bandwidth set to $B=5$ mHz. No special care was taken in cabling outside the rack. The goal was to observe the behaviour of the equipment operating in the field (not in a laboratory!), without counteracting against any incidental disturbing factor such as temperature variations, vibrations, etc., which may take place in normal operation.

Two sequences of TE data were acquired by measuring the output of the SSU with the sampling period $\tau_0=60$ ms. The sequence length was $N=90000$, with the SSU operating in locked mode, and $N=60000$, with the SSU operating in free running mode, thus covering a total duration respectively of $T=5400$ s and $T=3600$ s.

The graph of fig. 5 shows the curves of the Allan deviation (shortly ADEV) and the modified Allan deviation (shortly MADEV), i.e. the square root of $\sigma_y^2(\tau)$ and $\text{mod } \sigma_y^2(\tau)$ respectively, computed from these sequences by means of the estimators defined in [4,5]. The upper two curves refer to ADEV results, while the lower two ones refer to MADEV. As far as the ADEV result is concerned, it is worthwhile noting the consistency with the main theoretical indications derived in sect. 4.1.

Similarly, the graph of fig. 6 shows the curves of time deviation (shortly TDEV), i.e., the square root of TVAR and TIE_{rms} , computed from the same data sequences. It is worthwhile noting that, as in the free running configuration the theory does not guarantee the convergence of TIE_{rms} for some kind of noise, the results reported in fig. 4.3 may be strongly dependent on the total duration of the TE sequence.

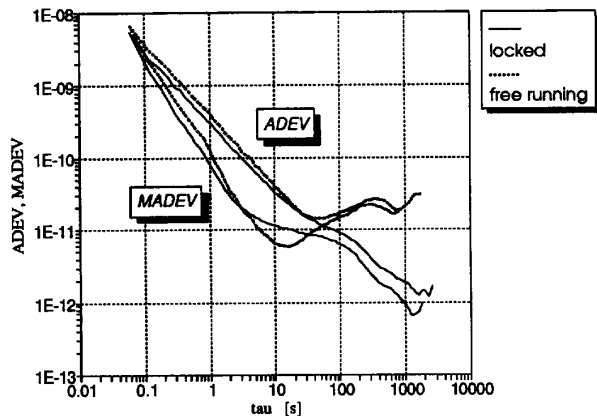


Fig. 5:
Comparison between free running clock and locked mode test configuration for ADEV and MADEV

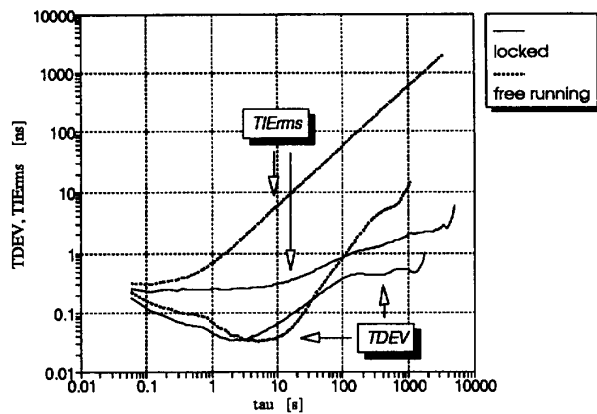


Fig. 6:
Comparison between free running clock and locked mode test configuration for TDEV and TIE_{rms}

According to our tests, when the time counter input signals $CK_{Ref}(t)$ and $CK_{Test}(t)$ are both 2.048 MHz sine waves, the total maximum peak-to-peak measurement error never exceeds 1 ns. This measurement error is mainly due to the so-called *trigger error*, i.e. the inaccuracy in detecting thresholds crossing of input signals, and is observable as a white PM noise added to the noise of the clock under test.

Unfortunately, this measurement noise, though very low, is not negligible as compared to the intrinsic clock noise, mainly in the short term, being the clock we studied a very high quality oscillator, and can be dominant for $\tau < 1$ s. Nevertheless, for the purpose of verifying the expected long term differences in the stability quantity behaviour between independent and synchronized configurations, the impact of measuring noise was not an issue.

5. Conclusions

Some important aspects of the evaluation and measurement of the most important frequency stability quantities defined in literature were examined, with particular emphasis on the impact of measurement configuration. Some indications stemming from the theoretical approach (waiting for an experimental validation) were confirmed, encouraging the efforts in pursuing on the way of timing signal and clock modelling as tool for good and efficient design of measurement schemes. The conceived experimental set-up, along with the post-processing software developed for the evaluation of the stability quantities, proved very useful both for the above mentioned validation and for gaining more insight into actual performance of timing supply devices.

Acknowledgment

The work of Marco Carbonelli, Domenico De Seta and Daniele Perucchini was carried out in the framework of the agreement between the Italian PTT and the Fondazione Ugo Bordoni

References

- [1] James A. Barnes, Andrew R. Chi, Leonard S. Cutler, Daniel J. Healey, David B. Leeson, Thomas E. McGunigal, James A. Mullen Jr., Warren L. Smith, Richard L. Sydnor, Robert F.C. Vessot, Gernot M.R. Winkler, "Characterization of Frequency Stability", IEEE Transactions on Instrumentation and Measurements, Vol. IM-20, No. 2, May 1971
- [2] J.Rutman, F.L. Walls, "Characterization of Frequency Stability in Precision Frequency Sources", Proceedings of the IEEE, Vol. 79, No. 7, July 1991, pp. 952-960
- [3] V.F.Kroupa, "Noise Properties of PLL Systems", IEEE Transactions on Communications, Vol. Com-30, No. 10, October 1982, pp. 2244-2252
- [4] M. Carbonelli, D. De Seta, D. Perucchini, "Clock stability measures for the assessment of synchronization network performance", Proceedings of SICON-ICIE'93, Singapore, September 1993
- [5] S.R. Stein, "Frequency and Time - Their Measurement and Characterization", in "Precision Frequency Control", Vol. 2, Academic Press, New York, 1985, pp.191-416
- [6] ITU-T Rec. G.811, "Timing Requirements at the Outputs of Primary Reference Clocks Suitable for Plesiochronous Operation of International Digital Links", Blue Book, 1988
- [7] M. Carbonelli, D. De Seta, D. Perucchini, "Some important issues related to Time Error definition and measurement", TSS 13 (former CCITT XVII), Geneva, July 1993
- [8] O. Brugia, M. Carbonelli, D. De Seta, D. Perucchini, "PLL bandwidth impact on slave clock output short term stability", European Transactions on Telecommunications (to appear)
- [9] M. Carbonelli, D. De Seta, D. Perucchini, "TIE_{rms} accumulation along slave clock chains", Proceedings of ICC'93, Geneva, May 1993, pp. 816-820
- [10] M. Carbonelli, D. De Seta, D. Perucchini, "Slave clock noise modelling for SDH synchronization network design: some results on clock chain performance", ETSI TM3, TD63, Bristol, October 1992