Impact of Slave Clock Internal Noise on Allan Variance and Root Mean Square Time Interval Error Measurements

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Abstract - Starting from a slave clock model, results describing the impact of clock internal noises on TIErms and ADEV are provided, based on theoretical analysis, computer simulations and experimental measurements. Comparison of the obtained results allows to validate the numerical approach used for calculations.

1 - INTRODUCTION

The introduction of Synchronous Digital Hierarchy (SDH) based networks [1] rises new important synchronization issues to be carefully investigated in order to exploit SDH capabilities: one major consequence is that network operators are facing the problem of designing a suitable synchronization distribution network. At present, hot issues, both in the scientific community and within the regulatory organisms, are the choice of meaningful quantities to characterize frequency stability and the impact of Slave Clock (SC) internal noises on the stability of timing signals. As far as the choice of stability quantities is concerned, in current regulations [2,3] three quantities, measured both in independent and synchronized clock configurations [4], have been adopted, namely the Maximum Time Interval Error (MTIE), the root mean square TIE (TIErms) and the Allan Variance (AVAR). While the behaviour and the performance of independent clocks is widely investigated in the literature [5,6,7], no extensive information and results are provided on the stability of timing signals distributed by SCs, as measured in synchronized configuration, even if this latter case is of primary importance in designing synchronization clock chains, in characterizing SC behaviour and in standardizing equipment performance. In this work, starting from a suitable SC model, results of numerical calculations describing the impact of SC noises on TIErms and AVAR are provided. Besides the theoretical analysis, time domain computer simulations of different SCs were run, whose results, enforced by some experimental verification, confirm the main conclusions derived from the clock model, validating, at the same time, the numerical approach.

2 - CLOCK STABILITY MEASURES

In the telecommunications field, a *clock* is a device able to supply a timing signal, ideally periodic,usable for the control of telecommunication systems. A mathematical model describing an actual timing signal $s(t)$ is given by [5-7] $s(t) = A\sin\Phi(t)$, where A is a constant amplitude coefficient and $\Phi(t)$ is the *total instantaneous phase* expressed by

$$\Phi(t) = 2\pi\nu_0 t + \pi D\nu_{nom}t^2 + \varphi(t) + \Phi_0,$$

in which ν_0 is the *initial frequency* of the clock; D is the *linear fractional frequency drift* rate; ν_{nom} is the *nominal frequency*; $\varphi(t)$ is the *random phase deviation* and Φ_0 is the initial phase.

The *Time function* $T(t)$ of a clock is defined, in terms of its total instantaneous phase, as $T(t) = \Phi(t)/(2\pi\nu_{nom})$. The *Time Error function* $x(t)$ of a clock generating a Time function $T(t)$, relative to a reference time $T_{ref}(t)$, is defined as $x(t) = T(t) - T_{ref}(t)$.

In the frequency domain, the model most frequently used to represent oscillator phase noise is the *power-law* model in which the spectral density $S_\varphi(f)$ of $\varphi(t)$ is described by a sum of terms, each varying as an integer power of the Fourier frequency

$$S_\varphi(f) = \sum_{\alpha=n_1}^{n_2} m_\alpha f^\alpha, \quad 0 \le f \le f_h; \qquad S_\varphi(f) = 0, \quad f > f_h, \qquad (1)$$

where n_1, n_2 and the m_α's are device dependent parameters and f_h, is an upper cut-off frequency. The most common noise types which dominate in precision oscillators are: White Phase Modulation (WPM), for α=0, Flicker PM (FPM), for α=-1, White Frequency Modulation (WFM), for α=-2, Flicker FM (FFM), for α=-3 and Random Walk FM (RWFM), for α=-4.

Time domain clock stability measurements are typically carried out based on methods which, using digital counters, allow to extract a sampled version of the function $x(t)$: the sequence of N values $x_n=x[t_0+(n-1)\tau_0]$, where t_0 is the initial observation time, τ_0 is the sampling period and n=1,2,...,N, is used to estimate the most important time domain stability quantities.

The two quantities that we consider, namely TIErms and Allan Deviation ADEV (i.e., the square root of AVAR), are spreadly used for the stability characterization of clock and timing signals. The estimators of TIErms and ADEV are expressed as follows

$$\text{TIErms}(\tau) = \sqrt{\frac{1}{N-n}\sum_{i=1}^{N-n}(x_{i+n} - x_i)^2}, \qquad (2)$$

$$\text{ADEV}(\tau) = \sqrt{\frac{1}{2n^2\tau_0^2(N-2n)}\sum_{i=1}^{N-2n}(x_{i+2n} - 2x_{i+n} + x_i)^2}, \qquad (3)$$

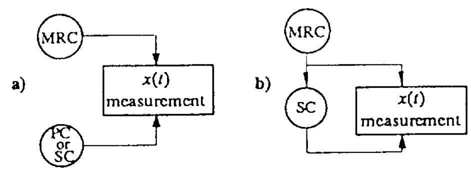
where $\tau = n\tau_0$ is the so called *observation interval*.

The following integral relationships between the phase noise PSD $S_\varphi(f)$ and each of the two quantities considered hold [5,7]

$$\text{TIErms}(\tau) = \sqrt{\frac{1}{(\nu_{nom}\tau)^2}\int_0^{f_h} S_\varphi(f)\sin^2(\pi f\tau)df}, \qquad (4)$$

$$\text{ADEV}(\tau) = \sqrt{\frac{2}{(\pi\nu_{nom}\tau)^2}\int_0^{f_h} S_\varphi(f)\sin^4(\pi f\tau)df}. \qquad (5)$$

As far as the characterization of a single autonomous (or slave) clock is concerned, two different measurement set-ups are actually of interest [4,7], as depicted in fig.1a and 1b.



MRC = Measurement Reference Clock ; SC = Slave Clock; PC = Primary Clock

Fig.1 - Configurations for clock stability measurements: a) independent clock configuration; b) synchronized clock configuration.

In the first one the timing signal from a Primary Clock (PC) (or from a free running SC) is matched against the output of a Measurement Reference Clock (MRC). In the second set-up, a SC is slaved to the output of the MRC, in order to evaluate the instabilities the SC adds to the reference timing signal while operating in locked mode. Both measurements are intended for in-lab assessment of autonomous or SC behaviour. The two configurations depicted in fig.1 can be described as follows.

• *Measurement of Time Error between Independent Clocks* (see fig.1a): this case occurs when each one of the two compared clocks

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operates independently of the other; in order to get meaningful measurement results, the MRC must be sufficiently better performing than the clock under test.

• *Measurement of Time Error between Synchronized Clocks* (see fig.1b): this case occurs when the two compared clocks are part of a synchronization distribution network and are traceable to a same master clock.

3 - Derivation of Theoretical Stability Measure Behaviour from a Noisy Clock Model

In our analysis we adopted the SC noise model shown in fig.2. This model, derived from a more general one proposed by Kroupa [8], was also used in [9] for evaluating the noise accumulation effects along SC chains.

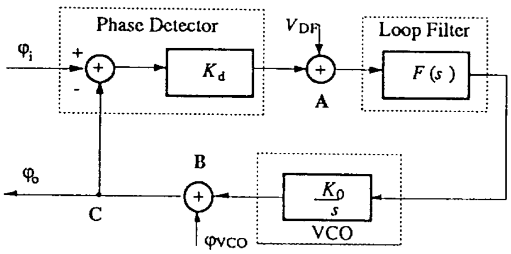

Fig.2 - Slave clock noise model.

The meaning of the quantities shown in fig.2 is as follows:

- φ_i [rad] and φ_o [rad] are the additive phase noises on the SC input and output signals respectively;
- φ_{VCO} [rad] is the phase noise due to the Voltage Controlled Oscillator (VCO);
- V_{DF} [V] is the voltage noise due to phase Detector and loop Filter (DF);
- K_d [V/rad] and K_0 [rad/(V·s)] are the phase detector and VCO gains respectively;
- $F(s)$ is the loop filter transfer function.

Internal noise processes φ_{VCO} and V_{DF} are characterized in terms of PSD, denoted as $S_{VCO}(f)$ and $S_{DF}(f)$ respectively. The *power-law* introduced in (1) was specialized as follows

$$S_{VCO}(f) = \frac{10^{-7}}{f^3} + \frac{10^{-6.75}}{f^2} + \frac{10^{-10.3}}{f} + 10^{-15.5} \quad [\mathrm{rad}^2/\mathrm{Hz}] \quad (6)$$

$$S_{DF}(f) = \frac{10^{-13}}{f} + 10^{-17} \quad [\mathrm{V}^2/\mathrm{Hz}], \quad (7)$$

$$f_h = 10^4 \text{ Hz}.$$

The chosen parameter values in (6) and (7) provide satisfactory models of random fluctuations in electronic devices and in commercial quartz crystal oscillators [8,9].

In order to evaluate phase noise PSD at the output of the SC, transfer functions $H(s)$, $H_A(s)$ and $H_B(s)$ between SC input, noise injection points (A and B in fig.2) and output (point C) are required. A very straightforward analysis yields the expressions

$$H(s) = \frac{K_0 K_d F(s)}{s + K_0 K_d F(s)},$$

$$H_A(s) = \frac{K_0 F(s)}{s + K_0 K_d F(s)} \quad [\mathrm{rad/V}], \quad H_B(s) = \frac{s}{s + K_0 K_d F(s)}$$

Assuming mutually uncorrelated noises, with amplitude small compared to the useful signals, superposition theorem can be used to derive the PSD $S_o(f)$ of total output noise φ_o. Since we are interested in evaluating the impact of internal noise sources only (i.e., φ_i=0) $S_o(f)$ is simply

$$S_o(f) = S_{DF}(f)|H_A(j2\pi f)|^2 + S_{VCO}(f)|H_B(j2\pi f)|^2 \quad [\mathrm{rad}^2/\mathrm{Hz}] \quad (8)$$

Substituting eqn.(8) for $S_\varphi(f)$ in eqns.(4) and (5), we can evaluate TIErms and ADEV behaviours for SCs: analytical calculation of such quantities, even for the simplest cases, proves quite cumbersome, and for some case seems unfeasible. For this reason a computer program using numerical integration algorithms was prepared to evaluate TIErms and ADEV. In order to assess the accuracy of our numerical computations, firstly we considered the case of a free running SC (see fig.1a): in this condition no filtering action is applied by the clock and it is quite easy to analytically derive closed forms [5] for the integrals in (4) and (5). The results obtained for this case are shown in figs.3 and 4: the solid lines represent the analytical results while different markers, for the various noise types considered, refer to numerical integration.

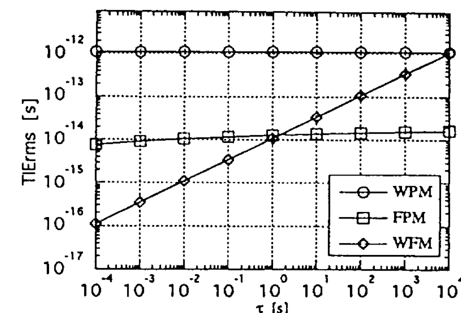

Fig.3 - Comparison of analytical (solid lines) and numerical (different markers) results for TIErms.

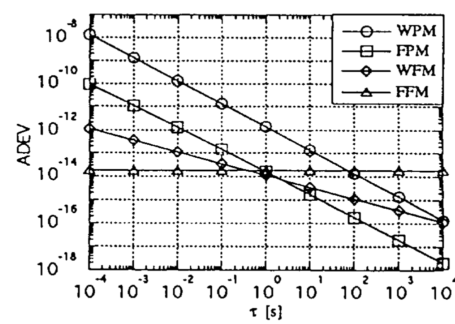

Fig.4 - Comparison of analytical (solid lines) and numerical (different markers) results for ADEV.

The above results demonstrate the excellent performance of the numerical algorithms adopted in our program and, as far as fig.4 is concerned, confirm the well known [5,7] behaviours of ADEV as a function of the noise types considered.

As a second case we considered the synchronized configuration of fig.1b. We adopted a lead-lag low-pass transfer function [10] for the loop filter and chose the other parameters as follows: ν_{nom}=2.048 MHz, K_d=1 [V/rad], K_0=6.28 [rad/(V·s)], SC bandwidth B=5 mHz, SC damping factor ζ=3. In order to simplify the analysis, the effects of the two noise sources (A and B in fig.2) were separately considered. In figs. 5 and 6 the results obtained taking into account the VCO noise only are reported: in these figures the dashed lines represent the results for each single noise component of eqn.(6) while the solid lines represent the composite behaviour. Comparing fig.3 with fig.5 and fig.4 with fig.6 the strong influence on TIErms and ADEV of the SC filtering action for observation intervals greater than $1/B$=20s is evident.

The results obtained considering the DF noise only are shown in figs.7 and 8: comparing these figures with figs.3 and 4, respectively, the influence of the SC filtering action is revealed for observation intervals smaller than $1/B$=20s.

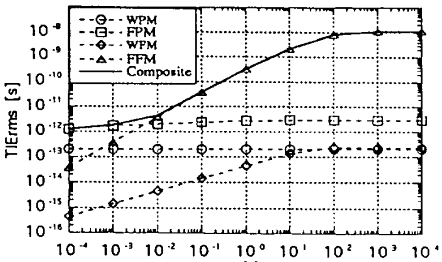

Fig.5 - Numerical analysis results for TIErms in the presence of VCO noise.

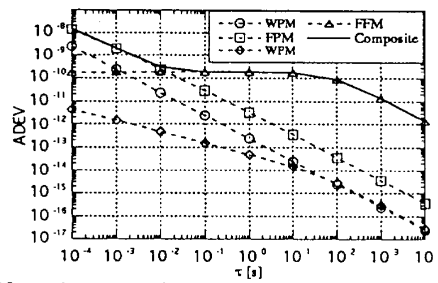

Fig.6 - Numerical analysis results for ADEV in the presence of VCO noise.

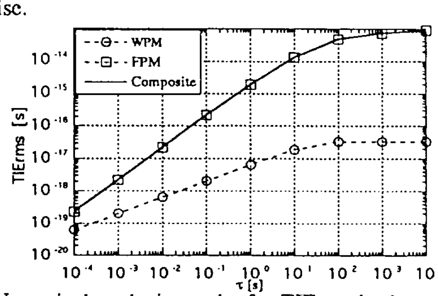

Fig.7 - Numerical analysis results for TIErms in the presence of DF noise.

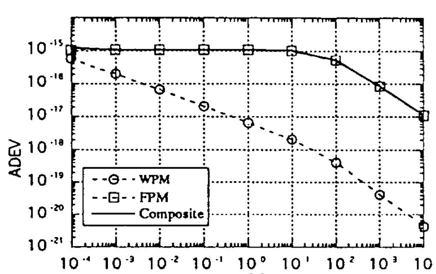

Fig.8 - Numerical analysis results for ADEV in the presence of DF noise.

4 - EVALUATION OF STABILITY MEASURES BEHAVIOUR BY COMPUTER SIMULATIONS

The derivation of theoretical behaviour of TIErms and ADEV in sect.3 was carried out in the frequency domain, based on the relationships (4) and (5). Experimental evaluation of stability measures is commonly performed in the time domain by means of estimators such as those expressed in eqns. (2) and (3). In order to derive useful information about the expected results of measurements as function of clock noise type, a computer based time domain simulation was attempted. First, two uniform pseudo-random noise sequences of length N=4096 were generated by means of a built in function of the mathematical CAD software used; then a Gaussian Pseudo-random Noise (GPN) sequence was obtained, based on a well known transformation formula [11], approximating a WPM noise. Finally, spectral shaping was applied by filtering the GPN sequence through a 1/2-order integrator [12] with transfer function $H_{1/2}(f)=(j2\pi f)^{-1/2}$ to obtain a FPM noise; repeatedly filtering through $H_{1/2}(f)$ yields WFM and FFM noises. Using the estimators (2) and (3) TIErms and ADEV were evaluated for the four noise sequences, getting the results shown in figs.9 and 10, respectively.

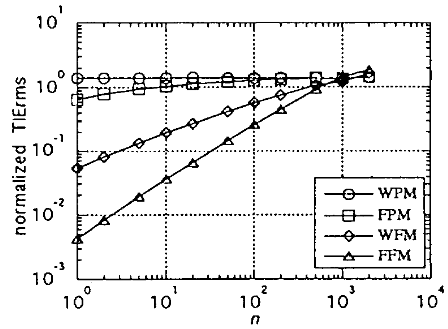

Fig.9 - TIErms simulation results.

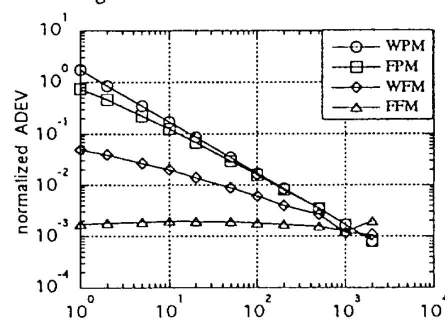

Fig.10 - ADEV simulation results .

Recalling the discussion in sect.3 these results can be interpreted as representing the stability of a free running clock. Further, to investigate the filtering action of the control loop operating when the clock is phase locked to an input reference, each of the four sequences was passed through a digitally simulated high-pass (HP) filter to obtain clock output phase noise due to a VCO noise source of that type; according to our clock model, only WPM and FPM noises were passed through a digitally simulated low-pass (LP) filter to obtain output phase noise due to a DF noise source. Calculation of (2) and (3) on these filtered sequences gave the results shown in figs.11 and 12, for the HP filtering case (normalized cut-off frequency f_c =0.01), and in figs.13 and 14, for the LP filtering case (f_c =0.01): these results confirm those obtained by the numerical calculation in the frequency domain, assuming that the fig.1b measurement configuration applies.

5 - ANALYSIS OF RESULTS

Examination of results from numerical calculations and measurement simulations allows to identify asymptotical behaviour of TIErms and ADEV for each type of internal noise which may affect clocks: in tab.1 these behaviours are reported in terms of suitable power-law type functions of τ, for TIErms and ADEV respectively. The case of unfiltered and HP filtered noise sources were considered for each of the four noise types, while for the case of LP filtered noise sources only WPM and PPM were evaluated, since these seem to be the noise types encountered in real PLL phase detectors and loop filters. Note that for the case of filtered noise, in general, two asymptotical laws can be identified: one applies at τ values definitely below $1/B$, the other at τ values much greater than $1/B$. This circumstance can actually play a significant role in differentiating free-running and locked SC noise performance.

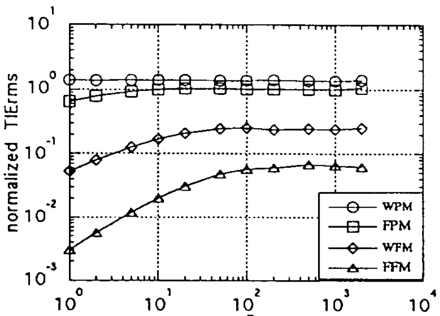

Fig.11 - TIErms simulation results for HP filtered sequences.

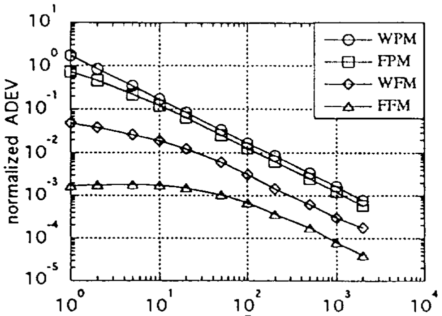

Fig.12 - ADEV simulation results for HP filtered sequences.

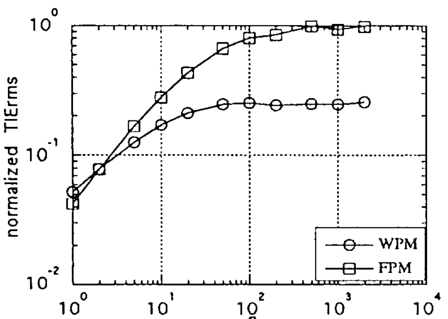

Fig.13 - TIErms simulation results for LP filtered sequences.

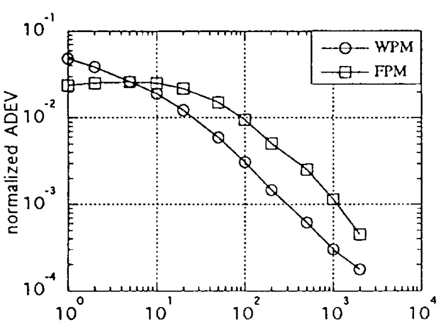

Fig.14 - ADEV simulation results for LP filtered sequences.

Table 1

	TIErms					ADEV				
Noise	No filter	HP filter		LP filter		No filter	HP filter		LP filter	
		$\tau<B^{-1}$	$\tau>B^{-1}$	$\tau<B^{-1}$	$\tau>B^{-1}$		$\tau<B^{-1}$	$\tau>B^{-1}$	$\tau<B^{-1}$	$\tau>B^{-1}$
WPM	τ^0	τ^0	τ^0	$\tau^{1/2}$	τ^0	τ^{-1}	τ^{-1}	τ^{-1}	τ^{-1}	τ^{-1}
FPM	$\approx\tau^0$	$\approx\tau^0$	τ^0	τ	$\approx\tau^0$	τ^{-1}	τ^{-1}	τ^{-1}	τ^0	τ^{-1}
WFM	$\tau^{1/2}$	$\tau^{1/2}$	τ^0	-	-	$\tau^{-1/2}$	$\tau^{-1/2}$	τ^{-1}	-	-
FFM	*	τ	τ^0	-	-	τ^0	τ^0	τ^{-1}	-	-

* Not analytically convergent; - Not calculated

Based on a high performance time counter, experimental measurements on the clock of a telephone exchange, having B=5 mHz, were performed. As an example, the ADEV measurement results are reported in fig.15, which confirm the main indications stemming from both the theoretical and simulation approaches.

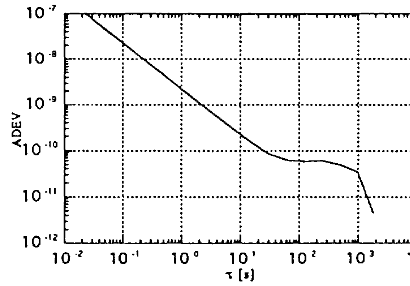

Fig.15 - ADEV experimental results.

6 - CONCLUSIONS

In this paper the impact of slave clock internal noise sources on the behaviour of stability measures was analyzed following both an analytical derivation approach and a simulation based time domain evaluation. Two well known stability measures, i.e., TIErms and ADEV, and both free-running and locked slave clock operation modes were considered. The good agreement between results of the two different approaches, enforced by some experimental confirmation, encourage the effort in pursuing on the way of clock modeling as a powerful tool for designing synchronization networks.

Acknowledgment - The work of M. Carbonelli, D. De Seta and D. Perucchini was carried out in the framework of the agreement between the Italian PTT and the Fondazione Ugo Bordoni.

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