System Architectures for Timing Transfer over PDH and SDH Transmission Networks

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Abstract: - In this paper, system architectures for point-to-point timing transfer over PDH and SDH transmission networks are detailed and discussed. First, it is pointed out that PDH transmission networks do not need to be synchronized, while they feature good timing transparency on transported tributaries. Then, schemes for point-to-point timing transfer over PDH and SDH transmission systems are discussed. The impact of modern network synchronization facilities including building clocks is also considered. The advantages of the SDH-based scheme with respect to the PDH-based scheme are highlighted. In conclusion, this paper provides a comprehensive and up-to-date overview on effective timing transfer architectures for synchronization distribution in modern digital networks, enabling the synchronization system engineer to implement the best technological solutions nowadays available.

Keywords: - clocks, digital communication, plesiochronous digital hierarchy, synchronization, synchronous digital hierarchy, timing.

1 Introduction

Network synchronization was at first an unknown issue, as not relevant to network operation and performance, but today plays a role of increasing importance in telecommunications, especially since transmission and switching turned digital [1][2].

The evolution of digital transmission and switching technology for the public telephone networks began with isolated digital transmission links between analog switching machines or analog radio transmission systems. The fact that digital technology was being used was transparent to the interfaces. Thus, there was no need to relate the internal clock rate in one system with the internal clock rate of another system.

Even as higher-level multiplexing systems were developed, there was no need of relating the clock rates of the higher-rate multiplexed signals with the clock rates of the lower rate tributaries. Indeed, transmission equipment based on Plesiochronous Digital Hierarchy (PDH) [3] does not need to be synchronized, since the bit justification technique allows multiplexing of asynchronous tributaries with substantial frequency offsets.

Problems began to arise with such asynchronous architecture when digital technology moved to switching machines too. Digital switching equipment requires to be synchronized in order to avoid slips at input elastic stores. And while slips do not affect significantly normal phone conversations, they may be troublesome indeed on some data services! The introduction of the circuit-switched data networks, therefore, yielded first the need of more stringent synchronization requirements.

In fact, however, the ongoing spreading of Synchronous Digital Hierarchy (SDH) [4] and SONET technology in transmission networks has really made synchronization a hot topic in standard bodies since the '90s. The need for adequate network synchronization facilities has become increasingly stringent in order to exploit fully SDH/SONET capabilities. It is widely recognized that SDH/SONET transmission may rely on a suitable and dependable timing distribution to fully meet all its benefits, in particular because pointer action may yield excess jitter on transported tributaries. For this reason, major network operators have set up national synchronization networks.

In this paper, system architectures for point-to-point timing transfer over PDH and SDH transmission networks are detailed and discussed. First, it is pointed out that PDH transmission networks do not need to be synchronized, while they feature good timing transparency on transported tributaries. Then, schemes for point-to-point timing transfer over PDH transmission systems, for synchronization of digital switches, are discussed. The impact of modern network synchronization facilities including building clocks is also considered. Finally, schemes for point-to-point timing transfer over SDH transmission systems are also discussed, highlighting their advantages with respect to the PDH schemes.

2 Timing Transparency of PDH Transmission Systems

PDH systems are based on bit justification [2], which allows multiplexing of asynchronous tributaries with substantial frequency offsets. Therefore, PDH transmission networks do not need to be synchronized. Every equipment clock is independent from the others, but their frequencies are just kept close to the nominal values within specified tolerance.

It is now important to point out that PDH systems are transparent to the timing content of transported digital signals. An E1 signal[1], multiplexed with other three asynchronous tributaries in an E2 and then so on in the upper PDH hierarchical level signals E3 and E4, once recovered at the end of the transmission chain has the *same* original average frequency as before the mux/demux chain.

In other terms, although the multiplexer clocks are independent, the transported signal keeps its average frequency, gathering only some jitter due to transmission lines and justification [2][5]. In fact, regardless of what multiplexing or demultiplexing may happen along the chain, no bits are added or deleted to or from the tributary bit stream along its path!

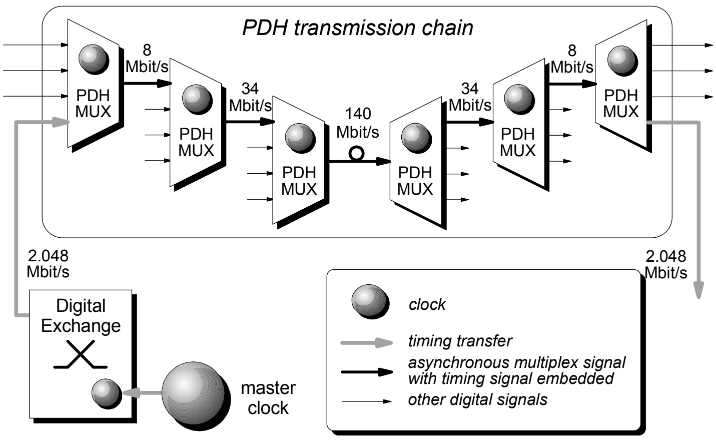

Fig. 1: Timing transparency through PDH transmission [1].

This property is remarkable indeed. The bit justification technique allows to *transfer the timing* content of a digital signal across a transmission chain where clocks are *asynchronous* instead, as shown in Fig. 1. There, grey thick links denote the signals that are synchronous with the master clock (i.e. transferring timing), while all the others are asynchronous. A 2.048 Mbit/s is generated by a digital switching exchange with the local clock driven by a master clock. The multiplex signals (black thick links) are not synchronous with it, but they embed, owing to bit justification, the 2.048 Mbit/s signal carrying timing. When the 2.048 Mbit/s is recovered, it is still synchronous with the master clock. Such a nice feature is exploited to transfer timing across PDH networks to synchronize clocks located in far locations.

[1] In this example and in the next ones, we refer for the sake of simplicity to the European PDH, but obviously the same considerations apply to the North-American PDH as well.

3 Synchronization of Digital-Switching Equipment via PDH Systems

Primary-rate multiplexers and digital-switching equipment, such as 64-kbit/s switching exchanges and cross-connects, do need to be synchronized, in order to avoid slips. On the contrary, PDH-transport networks do not need synchronization, because bit justification allows accommodating rate differences among signals. This role of network synchronization in digital switching networks with PDH transport infrastructure is expressed in Fig. 2.

Timing is commonly transferred across PDH links, exploiting their timing-transparency property, as said in the previous section (cf. Fig. 1).

The scheme of synchronization of two digital switching nodes (e.g., exchanges) through a PDH transmission chain is outlined in Fig. 3, where the same graphical notation of Fig. 1 holds: spheres are clocks, grey thick links denote signals transferring timing, black thick links are asynchronous multiplex signals with timing signal embedded and thin links are other digital signals.

The clock of the first exchange is enslaved to a master clock (e.g. the master clock of the whole digital exchange network) so that all the 2.048 Mbit/s signals output by this exchange are synchronous. The equipment clock of the second exchange is synchronized by means of one of these 2.048 Mbit/s (which may carry normal payload as well) assigned to transfer timing, which is transported across a PDH transmission chain from the first exchange to the second, multiplexed together with other signals.

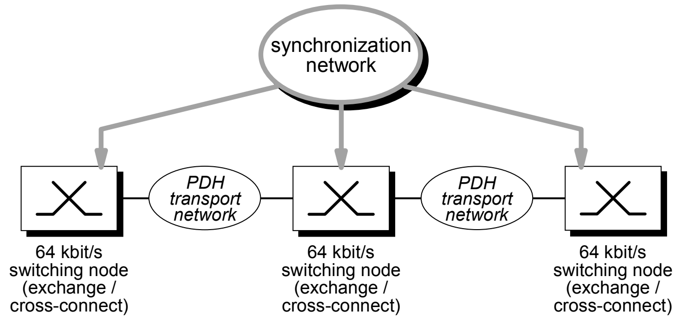

Fig. 2: Synchronization of digital-switching equipment with PDH transport infrastructure.

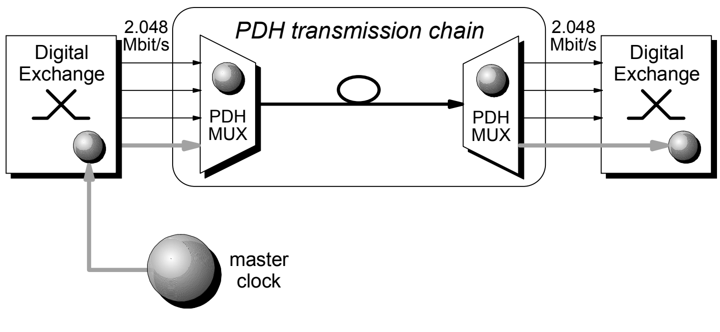

Fig. 3: Synchronization of two digital switching exchanges through a PDH transmission chain [1].

In case the digital switching network is served by a synchronization network, the scheme above becomes

slightly different. Modern synchronization networks are based on the concept of *building clock*. This is a slave clock which serves an entire office building by supplying timing to all the equipment deployed there, including digital switching exchanges, digital cross-connects and in case terminal equipment and multiplexers.
Such clocks are referred to as *Synchronization Supply Units* (SSU) or *Stand-Alone Synchronization Equipment* (SASE) in the ITU-T [6][7] and ETSI [8] standards, while they are known as *Building Integrated Timing Supplies* (BITS) in North America (ANSI standards).

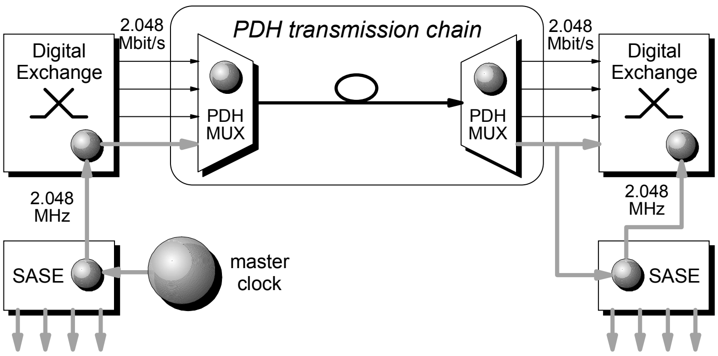

Fig. 4: Synchronization of two digital switching exchanges served by SASE clocks through a PDH transmission chain [1].

This latter scheme is outlined in Fig. 4. The clock of the first digital switching exchange is synchronized by the local building clock (SASE), synchronized by the master clock and distributing timing to the equipment of the first office building. Signals for intra-office timing distribution are usually analog 2.048 MHz signals, according to ITU-T Rec. G.703 [9]. The clock of the second exchange is not directly enslaved to a 2.048 Mbit/s transported through the PDH transmission chain. Conversely, the 2.048 Mbit/s carrying timing is used to synchronize the SASE clock that supplies timing to the equipment of the second office building, including the switching exchange.
The above schemes are currently the most applied world-wide to synchronize digital exchanges connected through PDH networks. Since the '70s, most telecommunications operators have set up national network synchronization plans, to control slips in digital switching exchanges and Digital Cross-Connects (DXC), which are mostly based on the two schemes above of point-to-point timing transfer from one digital exchange to another.

4 Synchronization of Digital-Switching Equipment via SDH Systems

Contrary to PDH, SDH[2] transmission takes advantage from network synchronization and may rely on it, in order to limit jitter and wander generation on output tributaries. Although some modern equipment overcomes such dependence with an enhanced design [2], yet the goal of guaranteeing jitter requirements at PDH/SDH boundaries [10] can be achieved only by an accurate synchronization of all the NEs aiming at avoiding any pointer action.
In networks using SDH for the transport infrastructure, therefore, it is necessary to synchronize not only primary-rate multiplexers and digital-switching equipment, but also the nodes of the SDH-transport networks. This role of network synchronization in digital switching networks with SDH transport infrastructure is thus expressed in Fig. 5.

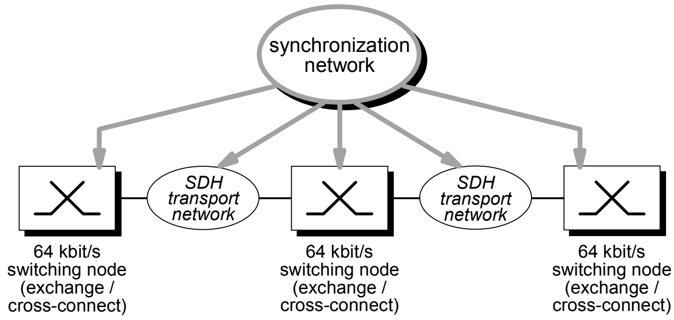

Fig. 5: Synchronization of digital-switching and transmission equipment with SDH transport infrastructure.

Nevertheless, timing transfer in SDH networks cannot follow the same schemes as with PDH. Contrary to what shown for PDH, in SDH networks it is definitely not advisable to carry timing on signals mapped in STM-*N* frames (e.g., 2.048 Mbit/s). The reason is that payload tributaries do not transport synchronization effectively, due to excess jitter exhibited in case of pointer justifications [2].
The best and most straightforward way to transfer timing in SDH networks is to carry it directly on the multiplex STM-*N* signals. The quality of the timing recovered from STM-*N* signals is the best achievable, as affected only by the line jitter (e.g. the jitter due to thermal noise and environmental conditions on the optical line) and not by bit justification or any other mapping issue.
The scheme of synchronization of two digital switching exchanges through a SDH transmission chain is outlined by Fig. 6. Also here, the same graphical notation of Fig. 1 holds: spheres are clocks, grey thick links denote signals transferring timing and thin links are other digital signals.
Unlike the previous section, only the scheme based on the availability of a synchronization network with SASE clocks in every office building has been considered here (cf. Fig. 4), as it is the standard solution for SDH synchronization networks [6][8].
The SASE clock in the first office building synchronizes not only the digital switching exchange clock, but also the SDH Equipment Clock (SEC), so that the output multiplex signal is now synchronous with the network master clock, contrary to what seen in the PDH case where the multiplex signal was asynchronous but embedding the signal carrying timing.

[2] In this section, for the sake of brevity, we will refer to SDH, which is the ITU-T standard designed as superset of the ANSI standard SONET. All principle considerations apply to SONET as well.

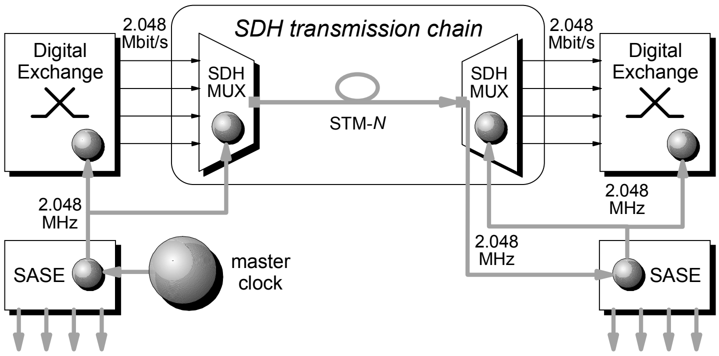

Fig. 6: Synchronization of two digital switching exchanges served by SASE clocks through a SDH transmission chain [1].

At the receiver side, the SEC is not directly locked to the incoming STM-*N* signal, as it might seem natural. A special function of the SDH equipment clock allows instead to extract timing from the incoming STM-*N* signal and to directly output it, not filtered, from the synchronization port as an ITU-T Rec. G.703 [9] 2.048 MHz signal, to synchronize the SASE of the second office building. This SASE distributes its timing to equipment of the office building, including the digital switching exchange and the SDH demultiplexer.

It is worthwhile noticing that this way of synchronizing the clocks of the second exchange may seem winding and unnecessarily complex, but it is definitely the best solution. Indeed, SASE clocks have much higher stability and filtering capabilities than simple SECs. Following this scheme, the clocks of the digital switching exchange and of the SDH (de)multiplexer in the second office building are synchronized by a timing signal which is much more stable. Moreover, if the STM-*N* signal should fail, the SASE guarantees a long-term output frequency in free-running operation, which is much more accurate than that one of the SEC.

5 Conclusions

In this paper, system architectures for point-to-point timing transfer over PDH and SDH transmission networks were discussed. The good timing transparency on transported tributaries of PDH systems was pointed out. The impact of modern network synchronization facilities including building clocks was also considered.

In conclusion, this paper provided a comprehensive and up-to-date overview on effective timing transfer architectures for synchronization distribution in modern digital networks, enabling the synchronization system engineer to implement the best technological solutions nowadays available.

References

[1] S. Bregni, *"A Historical Perspective on Network Synchronization"*, IEEE Communications Magazine, vol. 36, no. 6, June 1998.

[2] S. Bregni, *"Synchronization of Digital Telecommunications Networks*". Chichester, UK: John Wiley & Sons, 2002. 512 pages.

[3] ITU-T Rec. G.702 *"Digital Hierarchy Bit Rates"*, Blue Book, Geneva, 1988.

[4] ITU-T Rec. G.707 "*Network Node Interface for the Synchronous Digital Hierarchy (SDH)"*, Geneva, March 1996.

[5] P. R. Trischitta, E. L. Varma, *"Jitter in Digital Transmission Systems"*. Norwood, MA: Artech House, 1989.

[6] ITU-T Rec. G.803 *"Architectures of Transport Networks Based on the Synchronous Digital Hierarchy (SDH)"* Sec. 8, Geneva, June 1997.

[7] ITU-T Rec. G.812 *"Timing Requirements of Slave Clocks Suitable for Use as Node Clocks in Synchronization Networks "*, Geneva, June 1998.

[8] ETSI EN 300 462 *"Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks"*. Part 1-1: *"Definitions and Terminology for Synchronization Networks"*. Part 2-1: *"Synchronization Network Architecture"*. Part 3-1: *"The Control of Jitter and Wander within Synchronization Networks"*. Part 4-1: *"Timing Characteristics of Slave Clocks Suitable for Synchronization Supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) Equipment"*. Part 5-1: *"Timing Characteristics of Slave Clocks Suitable for Operation in Synchronous Digital Hierarchy (SDH) Equipment"*. Part 6-1: *"Timing Characteristics of Primary Reference Clocks"*.

[9] ITU-T Rec. G.703 *"Physical/Electrical Characteristics of Hierarchical Digital Interfaces"*, Blue Book, Geneva, April 1991.

[10] ITU-T Recs. G.823 *"The Control of Jitter and Wander within Digital Networks which are Based on the 2048 kbit/s Hierarchy"*, G.824 *"The Control of Jitter and Wander within Digital Networks which are Based on the 1544 kbit/s Hierarchy"*, G.825 *"The Control of Jitter and Wander within Digital Networks which are Based on the Synchronous Digital Hierarchy"*, Geneva, March 1993.