

Personal information

First name / Surname **Luca Fossati**
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Nationality Italian
Date of birth 22 April 1982
Gender Male
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Work experience

Dates	4 January 2010 - present
Occupation Held	Microelectronic Engineer
Employer	European Space Research and Technology Center, ESA-ESTEC (Noordwijk, The Netherlands)
Dates	1 January 2009 - 31 December 2009
Occupation Held	Active development and management of the contract with the European Space Agency for the development of simulator models of the LEON3 and LEON2 processors
Dates	20 September 2009 - 31 December 2009
Occupation Held	Teaching Assistant for the "Computer Architecture and Operating Systems" course
Employer	Politecnico di Milano (Milan, Italy)
Dates	November 2008 - January 2009
Occupation Held	Professor for the "Scientific Programming in C++" course
Employer	Collegio di Milano (Milan, Italy)
Dates	1 September 2008 - 31 January 2009
Occupation Held	Laboratory teacher for the "Fondamenti di Informatica" course
Employer	Politecnico di Milano (Milan, Italy)
Dates	1 September 2008 - 31 January 2009
Occupation Held	Laboratory teacher for the "Informatica B" course
Employer	Politecnico di Milano (Milan, Italy)
Dates	1 September 2007 - 30 May 2008
Occupation Held	Contractor for the Microelectronic Section
Employer	European Space Research and Technology Centre (ESTEC) (Noordwijk, The Netherlands)
Activities	<ul style="list-style-type: none">- Management and coordination of the development of ReSP (SystemC based Virtual Platform)- Modifications to the eCos Operating System to add Symmetric Multi-Processing support for the ARM target- Adaptation of the GNU/binutils software for the integration with ReSP- Benchmarked the ESA-funded GINA processor, 4-core LEON3 architecture- Participated to the definition of the architecture requirements for the "Next Generation Space Microprocessor" (NGMP)
Dates	1 March 2007 - 1 June 2007
Occupation Held	Teaching Assistant for the "Informatica Generale course" (introduction to computer science)
Employer	Politecnico di Milano (Milan, Italy)

Dates	1 November 2006 - 31 December 2006
Occupation Held	Contractor
Employer	Politecnico di Milano (Milan, Italy)
Activities	Enhancement of the PandA tool to lay the foundation for an autoparallelizing compiler (work developed in the context of the hArtes European Project)
Dates	1 October 2006 - 31 January 2007
Occupation Held	Laboratory tutor for the "Informatica 1" course
Employer	Politecnico di Milano (Milan, Italy)
Dates	1 March 2006 - 30 June 2006
Occupation Held	Laboratory tutor for the "Software Engineering" course
Employer	Politecnico di Milano (Milan, Italy)

Education and training

Date	20 February 2009
Mark	Obtained the qualification for the engineering in computer science profession 100/100
Dates	2007 - 2009
Research Interests	Ph.D. Student Multi-Core and Multi-Processor Systems - Electronic System Level Design Methodologies - Autoparallelizing Compilers - Embedded Operating Systems - Genetic Algorithms
Ongoing Projects	- ReSP (Reflective Simulation Platform): Virtual Platform based on Python and SystemC for the High Level modeling on Multi-Processor Systems-on-Chip. The project is being developed in cooperation with the European Space Agency. A team of 1 Research Fellow, 1 Ph.D. student, and several graduate students is cooperating on this project. - Zebu: autoparallelizing compiler. The work is part of the hArtes FP6 European Project - TRAP (TRansactional Automatic Processor generator): automatic generator of retargetable Instruction Set Simulators starting from high level abstract descriptions
Institution	Politecnico di Milano (Milan, Italy)
Dates	2005 - 2007
Title Awarded	Master Of Science in Computer Science
Graded Point Average	4.00/4.00
Topic of the thesis	<i>Development of a multi-processor simulation platform</i> The work involved, among other things, the implementation of both a functional and cycle accurate model of the ARM7TDMI processor and the implementation of a small Multi-threaded Multi-processor OS
Institution	University of Illinois at Chicago (Chicago, Illinois)
Dates	2004 - 2006
Title Awarded	Second Level Degree in Engineering in Computer Science
Final Mark	110/110 summa cum laude
Topic of the thesis	Development of a multi-processor simulation platform
Institution	Politecnico di Milano (Milan, Italy)
Dates	2001 - 2004
Title Awarded	Degree in Engineering in Computer Science
Final Mark	110/110 summa cum laude
Topic of the thesis	Implementation on an FPGA of an MPEG like compressor/decompressor.
Institution	Politecnico di Milano (Milan, Italy)
Dates	1996 - 2001

Title Awarded High School Degree
 Final Mark 98/100
 Institution Liceo Scientifico Elio Vittorini (Milan, Italy)

Additional work experience

Dates 1 January 2007 - Today
 Occupation Held Reviewer for International Conferences (DATE, CODES+ISSS, DAC) and for Journals (IEEE Transactions on Very Large Scale Integration Systems, IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems)
 Member of the Program Committee for the "NASA/ESA Conference on Adaptive Hardware and Systems" (AHS) for year 2010

Dates 24 July 2002 - 15 August 2002
 Occupation Held Activity Leader
 Employer English Summer Camp (London, UK)

Dates 20 June 2000 - 15 August 2000
 Occupation Held Activity Leader
 Employer English Summer Camp (Cirencester, UK)

Personal skills and competences

Mother tongue

Self-assessment
 European level^(*)

English

Italian

Understanding				Speaking				Writing	
Listening		Reading		Spoken interaction		Spoken production			
C2	Proficient user	C2	Proficient user	C2	Proficient user	C2	Proficient user	C2	Proficient user

^(*)Common European Framework of Reference (CEF) level

Computer competences Deep knowledge of *C/C++*, *Python*, *Java* programming languages and of the Java Environment in general; good knowledge of *C#* and *VHDL*
 Deep knowledge of *assembly language* for ARM and SPARC processors
 Deep knowledge of the structure of *ARM7*, *LEON2*, and *LEON3* processors
 Good knowledge of relational databases and of the *SQL* language
 Deep knowledge of the hardware modeling library *SystemC*; good knowledge of the graphical library *OpenGL*
 Deep knowledge of the *GNU/Linux* and *Microsoft Windows* operating systems
 Deep knowledge of the *eCos* operating system for embedded architectures; good knowledge of *RTEMS*

Other competences Good Communication and interpersonal skills have been necessary in all the professional experiences
 The ability to work in a team and to coordinate it has been developed during the Ph.D. studies and the related activities
 Capacity of working under pressure was acquired during Ph.D. studies and at the European Space Agency

Hobbies

Volleyball (played at a semi-professional level for 7 years), Biking, Hiking and Climbing, Digital photography

Publications

Books

LUCA FOSSATI. *MPSoC Analysis and Design: A Simulation Point of View*. Number 978-3639010091. VDM VERLAG DR. MULLER, 2009

International Journals

G. Beltrame, L. Fossati, and D. Sciuto. Resp: A nonintrusive transaction-level reflective mpsoC simulation platform for design space exploration. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 28(12):1857–1869, Dec. 2009

Giovanni Beltrame, Luca Fossati, and Donatella Sciuto. Decision-theoretic design space exploration of Multi-Processor platforms. *IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems*, 2010

International Conferences

Fabrizio Ferrandi, LUCA FOSSATI, Marco Lattuada, Gianluca Palermo, Donatella Sciuto, and Antonino Tumeo. Automatic Parallelization of Sequential Specifications for Symmetric MPSoCs. *International Embedded Systems Symposium 2007 (IESS '07)*, pages 179–192, 2007

G. Beltrame, C. Bolchini, L. FOSSATI, A. Miele, and D. Sciuto. A Framework for Reliability Assessment and Enhancement in Multi-Processor Systems-On-Chip. *DFT '07: Proceedings of the 22nd IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems (DFT 2007)*, pages 132–142, 2007

Fabrizio Ferrandi, LUCA FOSSATI, Marco Lattuada, Gianluca Palermo, Donatella Sciuto, and Antonino Tumeo. Partitioning and Mapping for the hArtes European Project. *Workshop on "Directions in FPGAs and Reconfigurable Systems: Design, Programming and Technologies for adaptive heterogeneous Systems-on-Chip and their European Dimensions" held during Design Automation and Test in Europe 2007 (DATE '07)*, April 2007

LUCA FOSSATI, Pier Luca Lanzi, Kumara Sastry, David E. Goldberg, and Osvaldo Gomez. A Simple Real-Coded Extended Compact Genetic Algorithm. *IEEE Congress on Evolutionary Computation 2007 (CEC 2007)*, pages pag. 342–348, 2007

C.A. Curino, L. Fossati, V. Rana, F. Redaelli, M.D. Santambrogio, and D. Sciuto. The Shining embedded system design methodology based on self dynamic reconfigurable architectures. pages 595–600, March 2008

Giovanni Beltrame, Cristiana Bolchini, LUCA FOSSATI, Antonio Miele, and Donatella Sciuto. ReSP: A Non-Intrusive Transaction-Level Reflective MPSoC Simulation Platform for Design Space Exploration. *Asia and South Pacific Design Automation Conference 2008 (ASP-DAC 2008)*, pages pp. 673 – 678, 2008 – Best Paper Candidate

Giovanni Beltrame and LUCA FOSSATI. ReSP: a design and validation tool for data systems. *DATA System In Aerospace (DASIA)*, 2008

G. Beltrame, L. Fossati, and D. Sciuto. High-Level Modeling and Exploration of Reconfigurable MPSoCs. *Adaptive Hardware and Systems, 2008. AHS '08. NASA/ESA Conference on*, pages 330–337, June 2008

Giovanni Beltrame, Luca Fossati, and Donatella Sciuto. Concurrency emulation and analysis of parallel applications for multi-processor system-on-chip co-design. pages 7–12, 2008 – Best Paper Candidate

Giovanni Beltrame, LUCA FOSSATI, and Donatella Sciuto. A Real-Time Application Design Methodology for MPSoCs. *Design Automation and Test in Europe (DATE)*, pages p. 767–772, 2009

Signature