



2PARMA Project

PARallel Paradigms and Run-time Management techniques for Many-core Architectures

HiPEAC Clusters Meeting, Chamonix, April 7th, 2011



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FP7-248716-2PARMA Project

List of Project Partners



1. Politecnico di Milano (POLIMI) – Italy
(Coordinator)



2. STMicroelectronics (STM) – Italy



3. Fraunhofer Institut for Telecommunications / Heinrich-Hertz Institut (HHI) – Germany



4. Interuniversitair Micro-Electronica Centrum (IMEC) – Belgium



5. Institute of Communication and Computer Systems (ICCS) - Greece



6. RHEINISCH-WESTFAELISCHE TECHNISCHE HOCHSCHULE AACHEN (RWTH) - Germany



7. Synopsys (CoWare) - Belgium

Project Coordinator

prof. Cristina SILVANO, POLIMI

Project Technical Manager

prof. William Fornaciari, POLIMI

Start date: January 1st, 2010

Project duration: 3 years

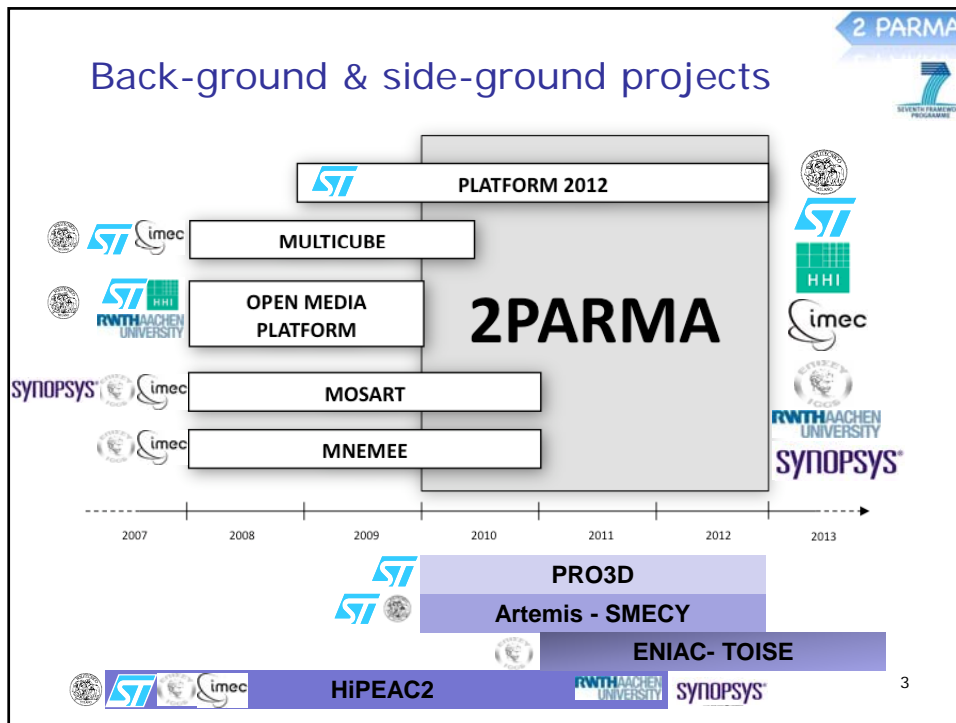
Total effort: 408 PM

EC Contribution: 2.74 M€

www.2parma.eu

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Scientific and Technical Objectives

Main Goals

- Programmability of Many-core Computing Fabrics
- Virtualisation and Continuous Adaptation
- Design Space Exploration
- Runtime Adaptivity

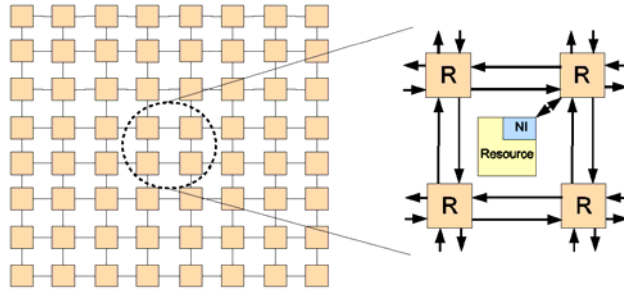
Project Outcomes

- Integrated Compiler Toolchain and OS Layer
- DSE Toolchain
- Run-time Resource Manager

The 2PARMA project focuses on the definition of suitable parallel programming models, instruction set virtualisation, run-time energy/power and resource management policies and mechanisms as well as design space exploration methodologies for Many-core Computing Fabrics.

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Many-Core Computing Fabric Template



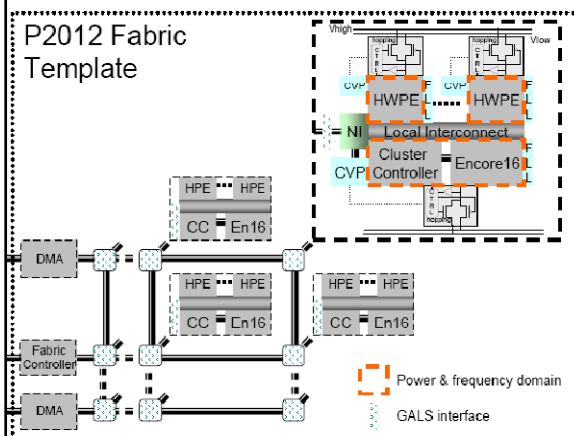
The 2PARMA project focuses on the flexible family of parallel and scalable computing processors, which we call **Many-core Computing Fabric Template**, composed of many processing cores interconnected by an on-chip network.

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Platform 2012: Scalable Architecture Template

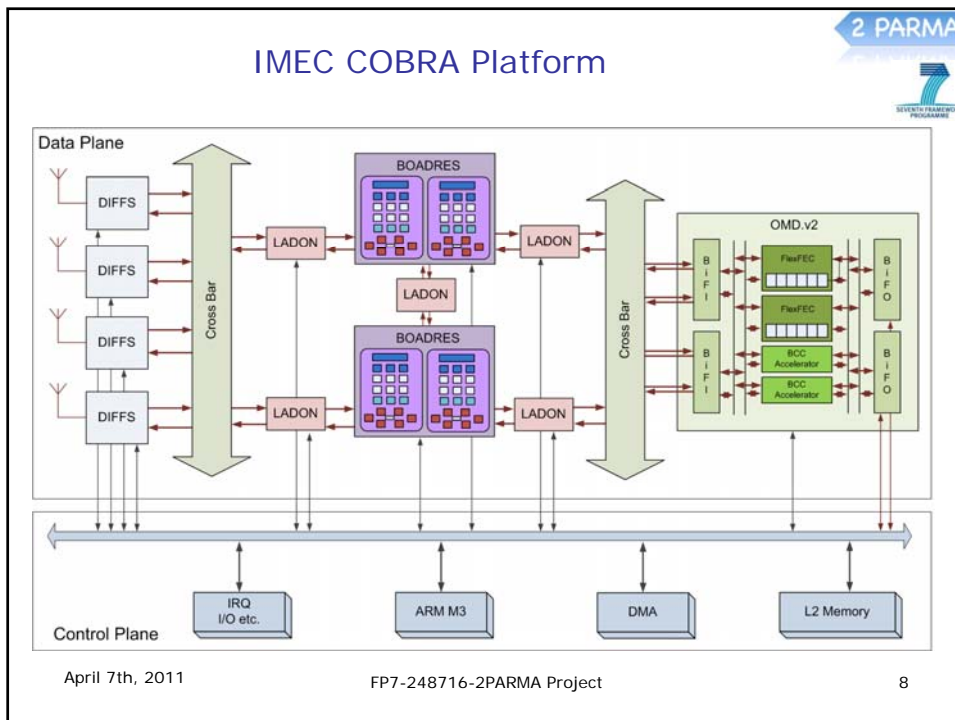
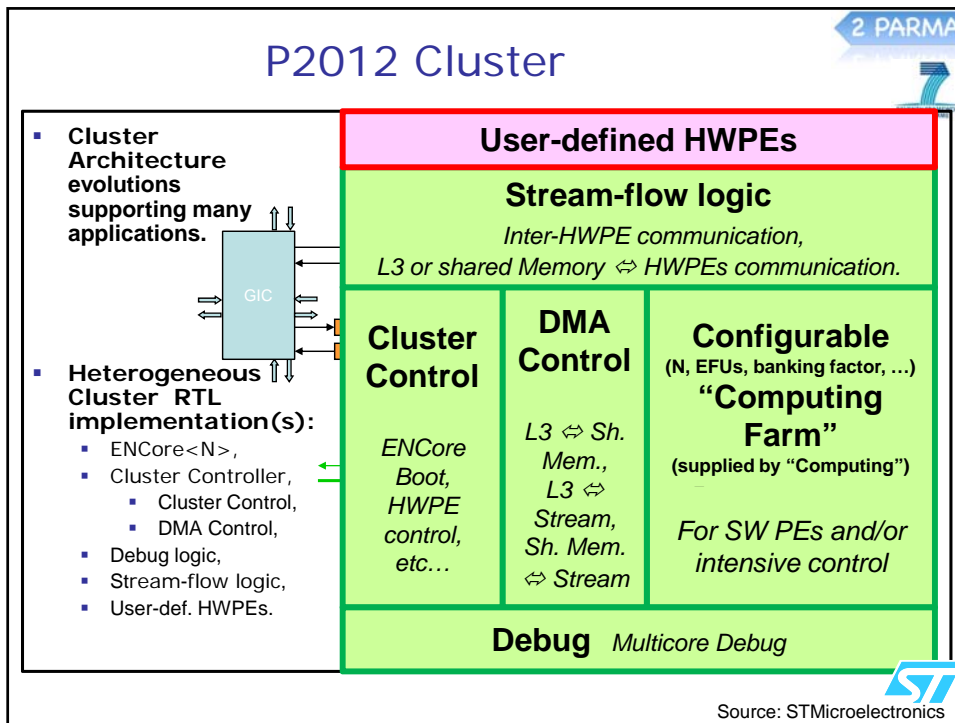


Platform 2012: A Many-core Programmable Accelerator for Ultra-Efficient Embedded Computing in Nanometer Technology

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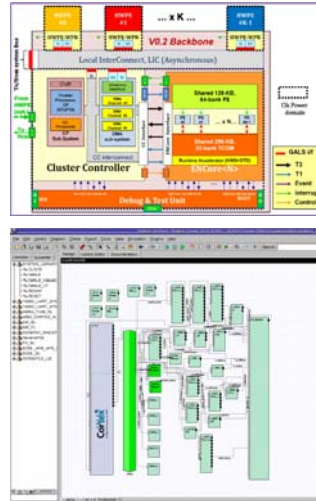
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Source: STMicroelectronics



Synopsys Virtual Platforms

1. Abstract model mimicking P2012 in support of CBSE methodology
2. ARM based multi-core platform supporting Linux OS for design tool validation
 - Integration with DSE tools
 - Investigate RTRM support



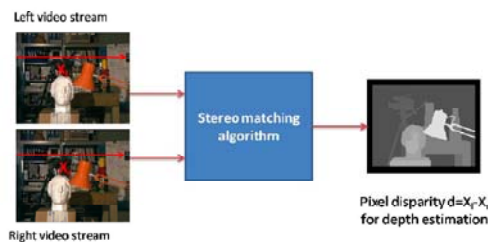
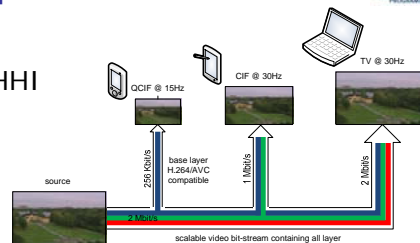
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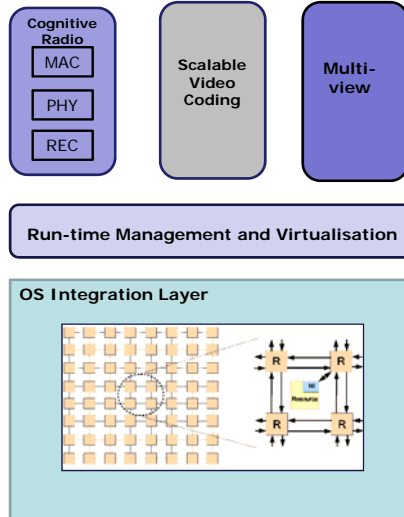
2PARMA Target Applications

- Scalable Video Coding (SVC) – HHI
- Cognitive Radio
 - Physical Layer – RWTH-ISS
 - MAC Layer – RWTH-iNETs
 - Reconfigurable Radio – IMEC
- Multi-view Image Processing - IMEC



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Applications/Architecture Integration

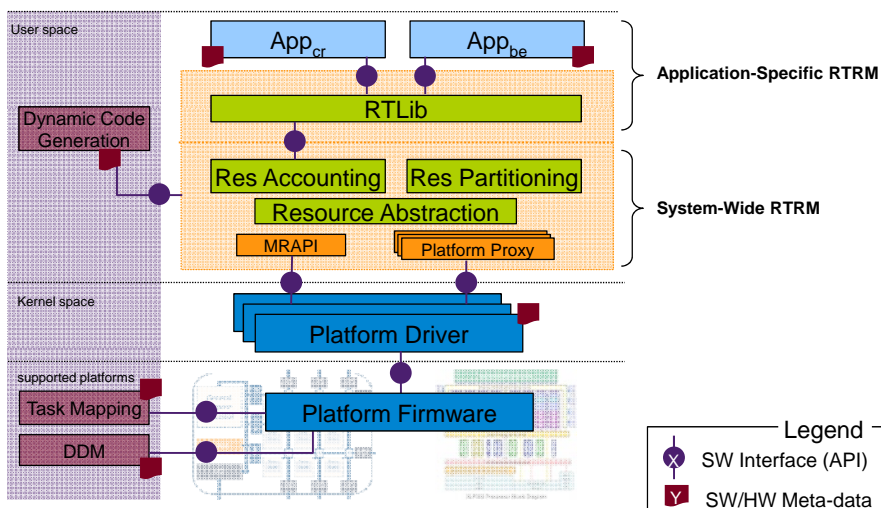


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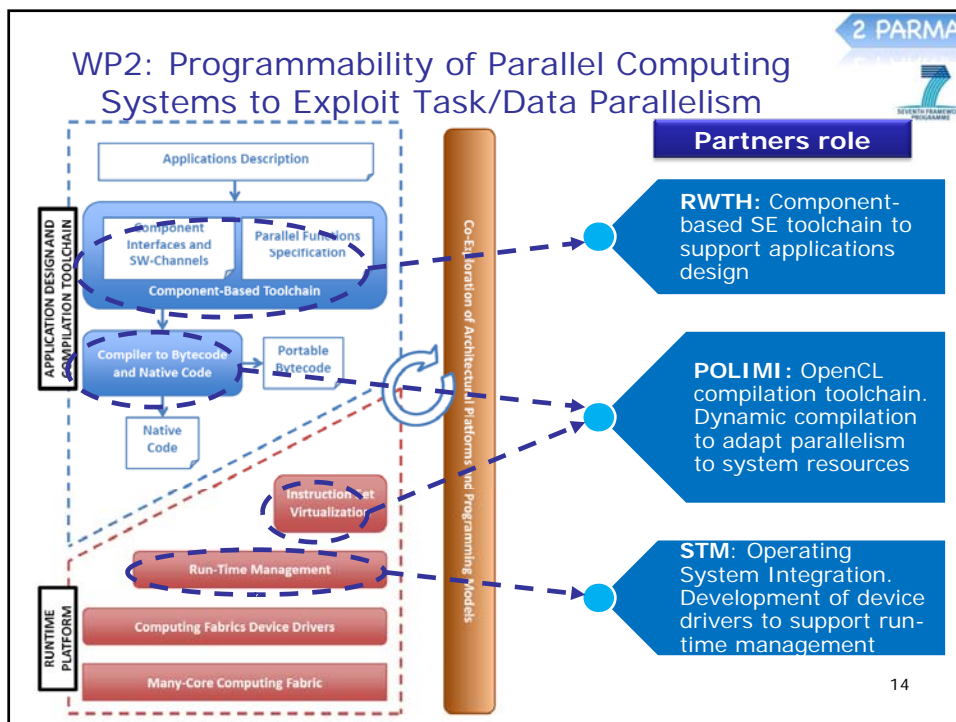
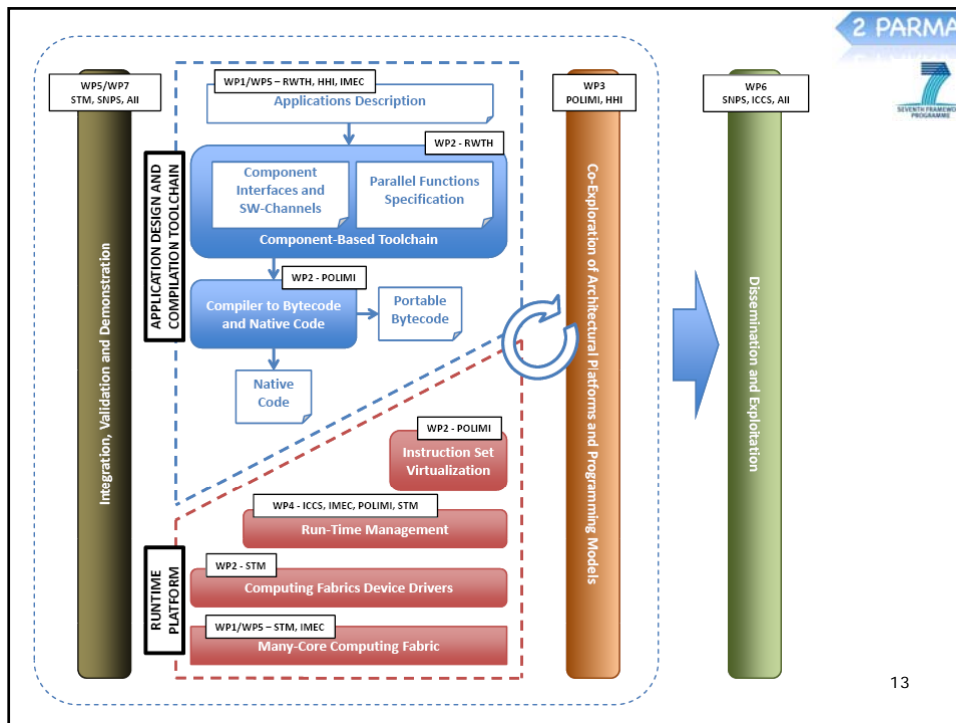
The 2PARMA Run-Time Resource Manager Overall view



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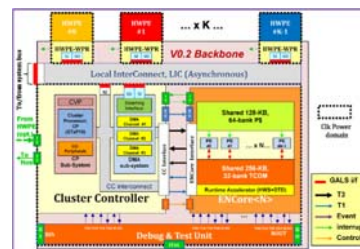
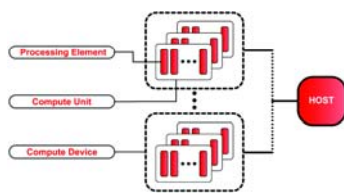


Mapping OpenCL to Computing Fabrics

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- Analysis of OpenCL programming model (strengths and weaknesses) vs P2012 Computing Fabric
- Specification of Computing Fabric-specific extensions to OpenCL
- Proposed OpenCL extensions targeting Computing Fabrics
- OpenCL front-end compilation toolchain for LLVM to be publicly released soon
- Dynamic compilation to adapt parallelism to system resources



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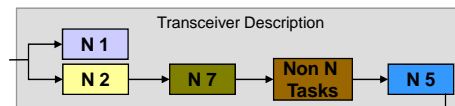
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Nucleus Methodology

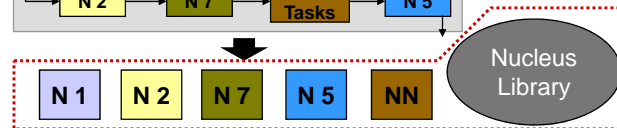
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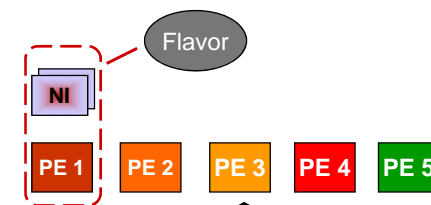
Transceiver Description



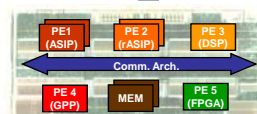
Nuclei



PEs

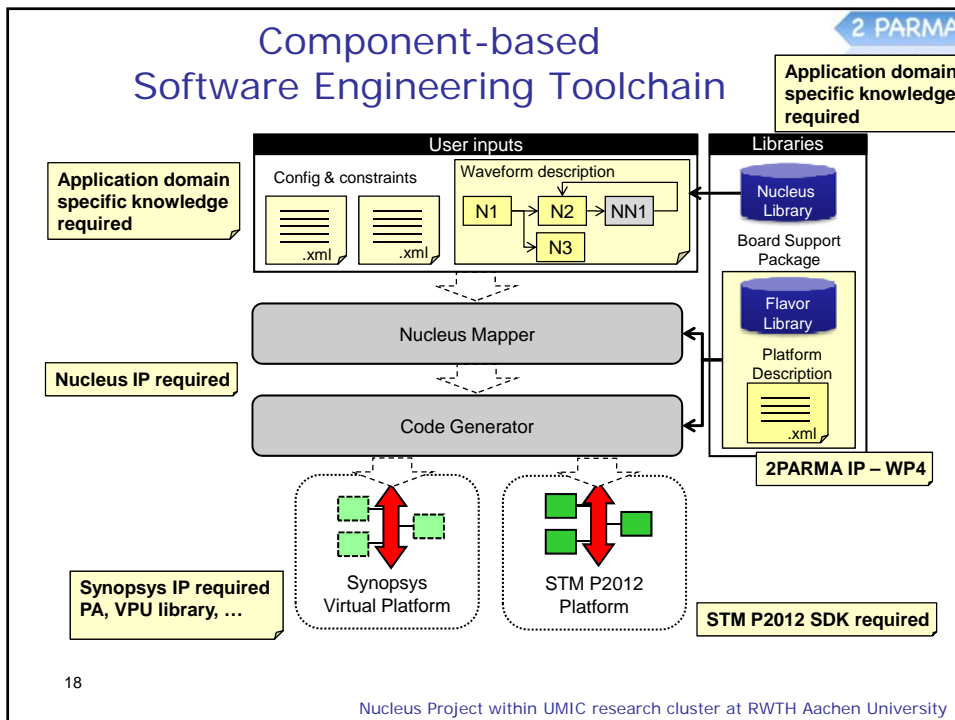
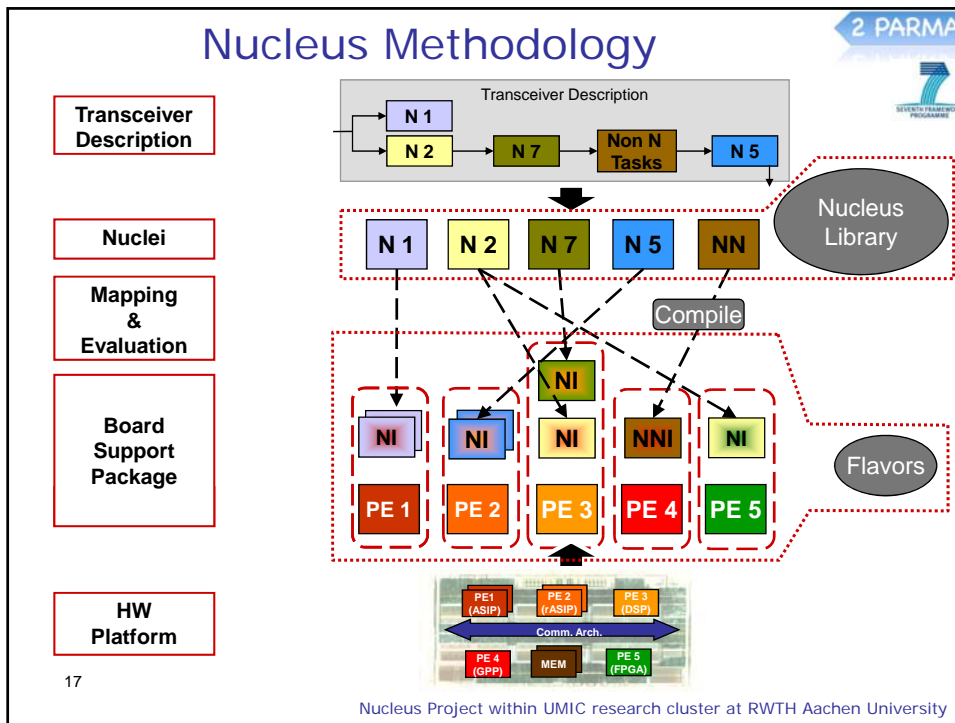


HW Platform



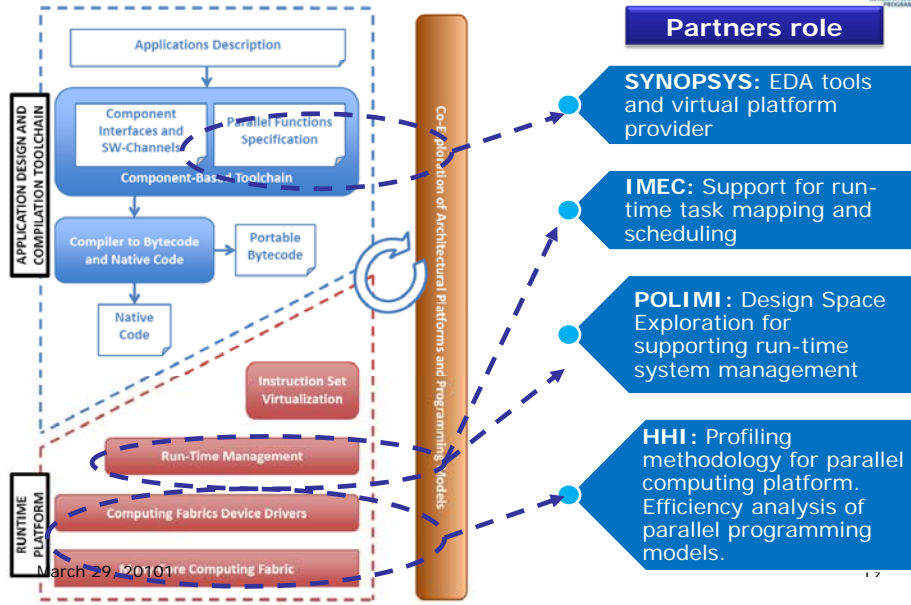
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Nucleus Project within UMIC research cluster at RWTH Aachen University



WP3: Co-exploration of Architectural Platforms and Programming Models

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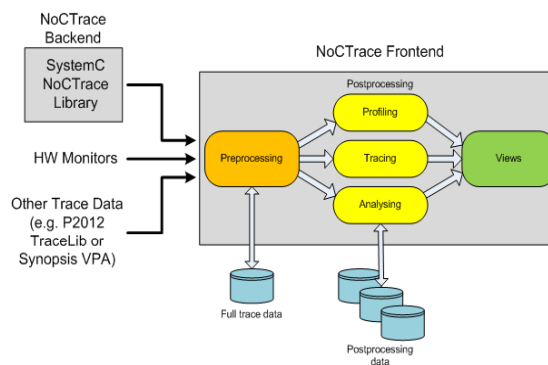


HHI NoCTrace Architecture

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- NoCTrace backend
 - collects data
- NoCTrace frontend
 - processes data
 - manages data (persistency)
 - presents data (GUI)



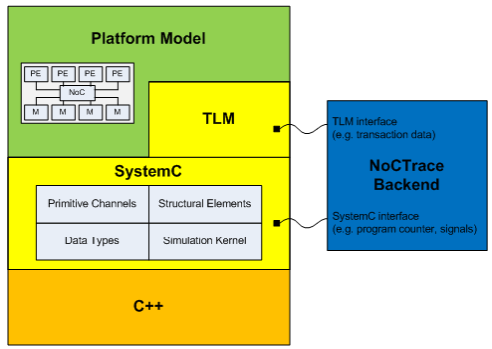
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HHI NoCTrace Backend

- Extract/record program counter and transaction data in SystemC kernel
- Perform automatic design analysis to get to know where to place the probes

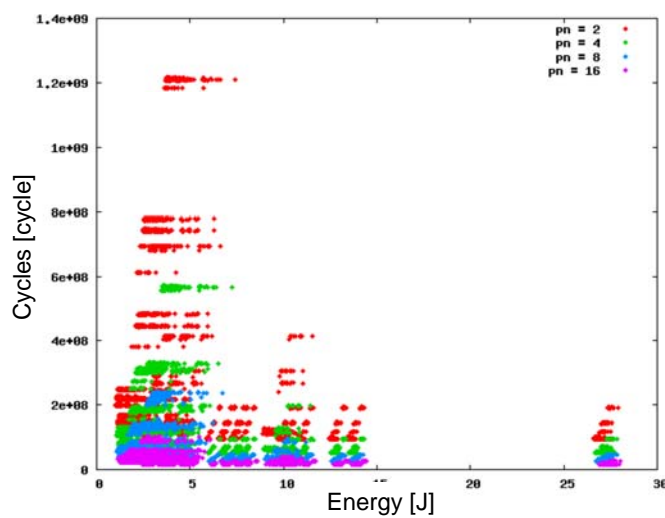


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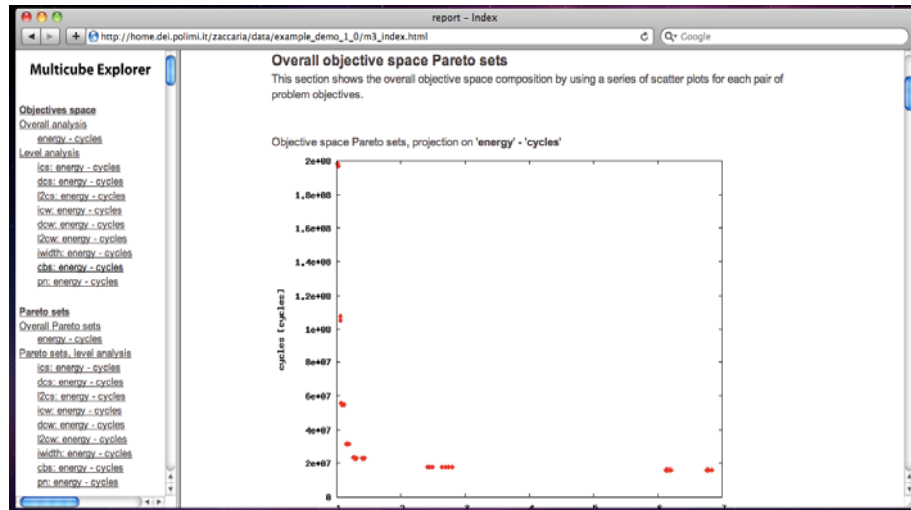
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Automatic Multi-Objective Design Space Exploration



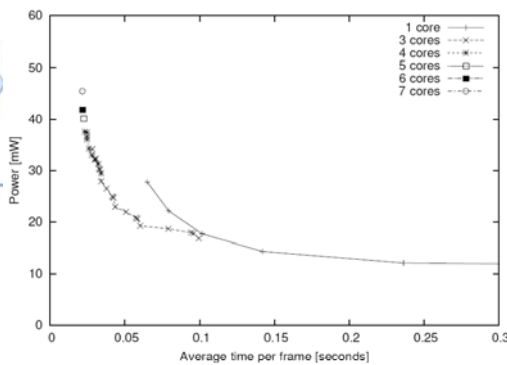
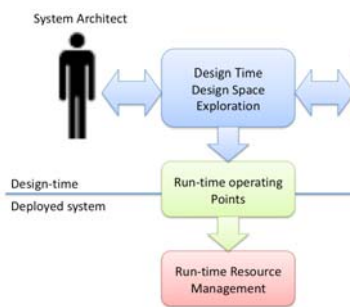
Source: Politecnico di Milano - MPEG2 decoder – MIPS-based multiprocessor – 70nm tech. node – 10 frames

Automatic Multi-Objective Design Space Exploration



Source: Politecnico di Milano - MPEG2 decoder, generated with Multicube Explorer

Design-time Exploration to support Run-time Resource Management

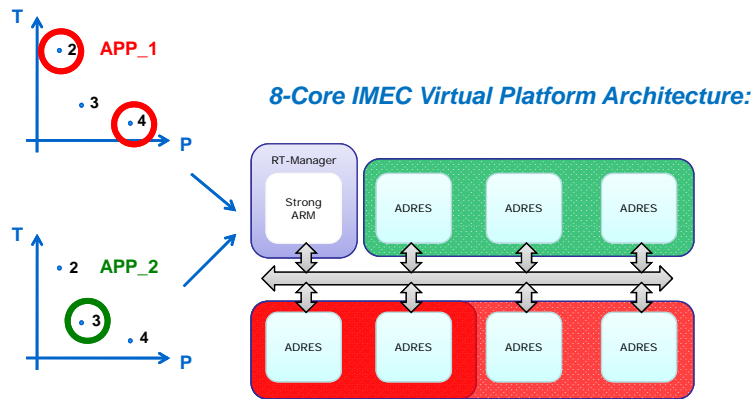


- Based on the **design-time exploration**, we derive a set of Pareto **operating points** corresponding to power, resources (number of cores) and QoS (average time per frame).
- The operating points will be used by the **Run-time Resource Manager** to achieve QoS requirements (average time per frame) while meeting overall resources (number of cores) and minimizing power consumption



Run Time Management of multi-core platform

- The system state can change due to some events:
 - A new application executed or
 - QoS requirements modified



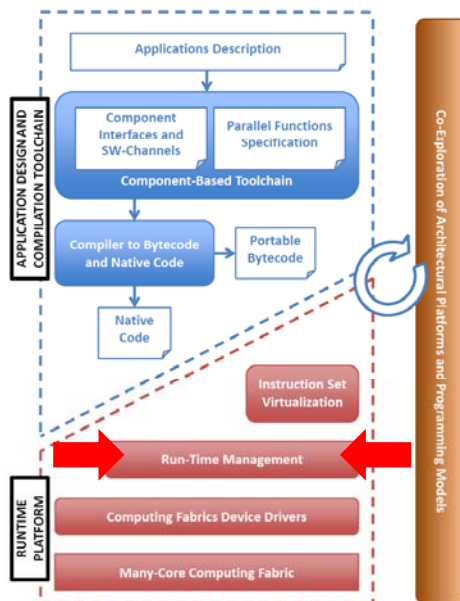
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WP4: Runtime Resource Management



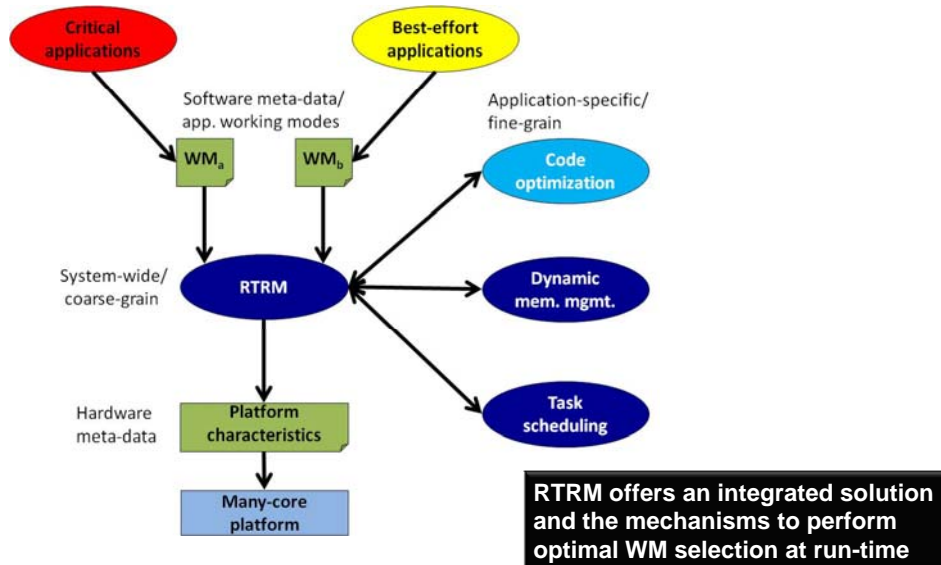
Partners role

- ICCS:** Adaptive dynamic data management
- IMEC:** Adaptive run-time task mapping and scheduling
- POLIMI:** Run-time QoS constrained resource and power manager at the OS-level
- STM:** Operating System Integration. Development of Device Drivers

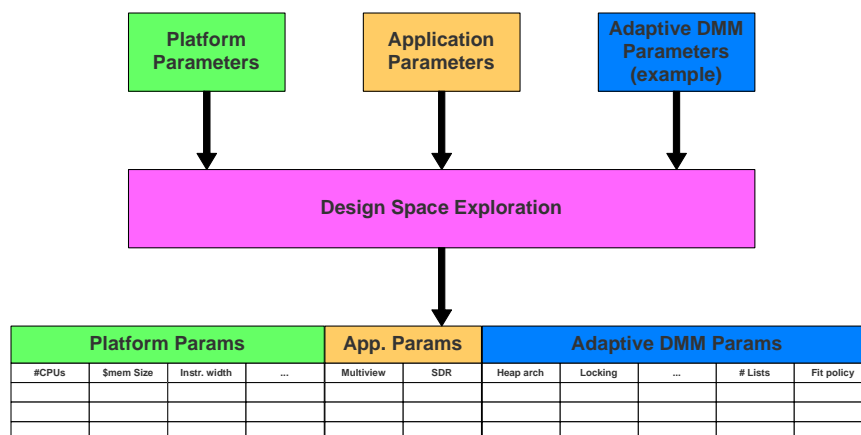
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Run-time resource management (RTRM): Overview



What is a working mode?

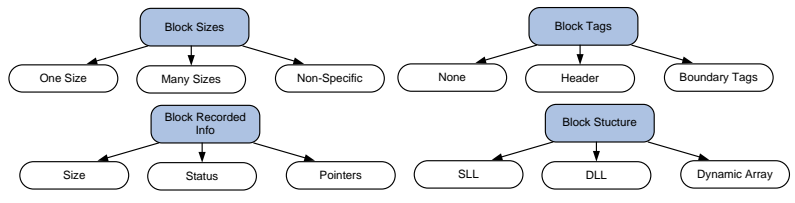




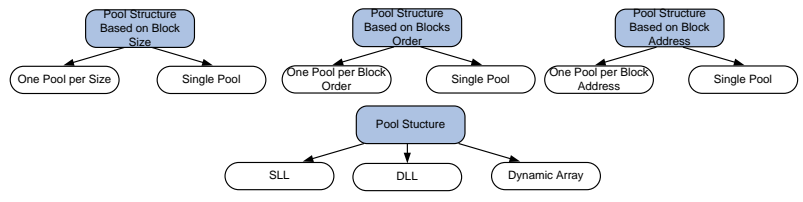
Example of Intra-Heap MTh-DMM Design Space

Intra-Thread Level Design Space

E. Block Structure Decisions



F. Pool Organization Decisions



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- Acronym: 2PARMA
- Title: PARAllel PARadigms and Run-time Management techniques for Many-core Architectures
- Project ID: FP7-ICT-2009-4-248716
- Project Duration: January 2010 - December 2012
- Project Coordinator: Prof. Cristina Silvano, POLIMI
- Project Technical Manager: Prof. William Fornaciari, POLIMI

Partners

The current trend in computing architectures is to replace complex superscalar architectures with small homogeneous processing units connected by an on-chip network. This trend is mostly dictated by inherent silicon technology frontiers, which are getting as closer as the process densities levels increase. The number of cores to be integrated in a single chip is expected to rapidly increase in the coming years, moving from multi-core to many-core architectures. This trend will require a global rethinking of software and hardware design approaches.

This class of computing systems (Many-core Computing Fabric) promises to increase performance, scalability and flexibility if appropriate design and programming methodologies will be defined to exploit the high degree of parallelism exposed by the architecture. Other potential benefits of Many-core Computing Fabric include energy efficiency, improved silicon yield, and accounting for local process variations. To exploit these potential benefits, effective run-time power and resource management techniques are needed. With respect to conventional computing architectures, Many-core Computing Fabric offers some customisation capabilities to extend and/or configure at run-time the architectural template to address a variable workload.

The 2PARMA project aims at overcoming the lack of parallel programming models and run-time resource management techniques to exploit the features of many-core processor architectures. To this purpose, a proper Consortium has been set up to gather the required expertise in the areas of system/application software and computing architectures.

The 2PARMA project focuses on the definition of a parallel programming model combining component-based and single-instruction multiple-thread approaches, instruction set virtualisation based on portable bytecode, run-time resource management policies and mechanisms as well as design space exploration methodologies for Many-core Computing Fabrics.

[2PARMA Publishable Summary for Year 1 (2010) (PDF Version)]

[2PARMA Project Fiche (PDF Version)]

[2PARMA Flyer (PDF Version)]

[2PARMA Poster (PDF Version)]

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