

RESEARCH STATEMENT

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1. RESEARCH NARRATIVE

My research activity is primarily focused on the area of **Computer Architectures** and **Computer Aided Design Methodologies**, with particular emphasis on the following research topics:

- *Power-aware computing for embedded systems*
- *Design space exploration of multi/many-core architectures*
- *Network-on-chip architectures*
- *Fault detection and fault tolerant coding techniques*

For each research topic, I first introduce the motivations behind the research and the major challenges which define the scope of my research to date. I then outline my main research directions across these research challenges before summarizing my research accomplishments. Finally, I outline my general research approach used across each of the research challenges and I present my research collaborations.

1.1. POWER-AWARE COMPUTING FOR EMBEDDED SYSTEMS

Challenges. The continuous growth of the integration level of microelectronic devices has led to the integration of a huge amount of transistor resources on a single chip. These resources can be exploited by computer architects to design increasingly complex systems providing massive parallelism and improved performance for computing applications. At the same time, computing devices have become more and more ubiquitous, and today's portable embedded systems integrate an enormous amount of computational resources into small form-factor devices. The rapid evolution of the microelectronic technology toward smaller mask-level geometries, leading to higher integration level and higher performance, is also motivating towards the integration of multi/many cores on a single chip. However, as manufacturing process technologies continue to shrink, severe technology scaling challenges arise. Minimizing energy consumption, while preserving performance, is one of these challenges. The demand of processors and more in general VLSI and ULSI circuits with low power features is steadily increasing in the digital systems market for a broad range of applications.

Power dissipation has been identified as the main performance limiter for high-performance processors, while power dissipation limits the capabilities of battery-powered embedded mobile devices and wireless sensor nodes. Modern low power electronic devices are also quite often characterized by tight performance constraints: power consumption must be minimized as well as high-end performance must be reached. The stringent power constraints are thus become contextual with performance constraints rather than facing each other. This trend is currently motivated by the demand for embedded mobile computing devices running medium or high-end software applications, such as streaming video encoding and decoding, for which the throughput constraint is strictly dependent on the relative power consumption of the device. In this context, the designer's intervention is essential for taking high-level architectural decisions and providing creative solutions, while the design synthesis, the efficiency and the quality of the overall process is usually carried out by a set of automatic CAD tools supporting power estimation and optimization. The crucial role of the designer is currently moving from design tasks at the lowest levels of abstraction to the highest levels of design evaluation and optimizations by considering, at the same time, power, performance and overall system cost. This approach is justified by the fact that operating at the highest levels of abstraction makes it feasible the early exploitation of several degrees of freedom by trading off accuracy and efficiency of power/performance estimations. Therefore, system designers are expecting much more advantages by affording the problem of power reduction from a high-level perspective.

My research on power-aware design started in 1996, at the beginning of my Ph.D. thesis work. The main goal is to develop design techniques for the phases of analysis and synthesis of digital circuits and systems to reduce the power consumption at the higher levels of abstractions. The research activity is mainly focused on two main areas: estimation and optimization of power

dissipation. The power optimization phase is much more effective once it is tightly connected to the power estimation phase to enlarge as much as possible the search space of design solutions and to maintain a good tradeoff between the accuracy and the efficiency of the power estimates.

1.1.1. High-Level Power Estimation

The first part of my Ph.D. thesis work involved the development of a power assessment framework from a system-level co-design perspective. The overall goal is to provide a model to evaluate the power consumption associated with the hardware and software modules as well as the HW/SW communication of a digital system. First, we define a methodology for both static and dynamic estimation of power consumption at the SW-level, to be integrated into a more general HW/SW co-design framework for embedded systems. This work copes with the definition of power evaluation metrics for the SW to be applied during or after the HW/SW partitioning phase. Second, the research work aims at defining a conceptual framework suitable for achieving accurate yet efficient estimation of the power consumption associated with the HW-bound part of digital systems. The work focuses on the HW components described at the highest levels of abstraction (behavioral or architectural) expressed in VHDL. The most relevant aspect of the proposed approach is to be quite general, since it considers a general System-on-Chip architecture, suitable for many industrial applications, as well as their single sub-parts, that typically constitute the HW-side of an embedded system. The model parameters considered in our analysis concern only the I/O behavior of the different HW modules, and they do not refer to the internal structure of the modules. The most important value added has been the introduction of a third dimension, power, to the speed versus area design space, where the architectural design exploration is usually carried out. The objective is to provide the designer the capability of analyzing and comparing different solutions in the architectural design space, before the synthesis task. As a matter of fact, relative power figures can be used to guide the designer in exploring the relative impact of the different design alternatives on the quality of the final design rather than to provide absolute power data. Experimental results derived from the application of the proposed model have shown the effectiveness of the approach as a relative power indicator. Third goal of the research is to provide a model to assess the power consumption due to system-level address and data buses, which represents one of the major contributions to the overall power budget. A model has been defined to evaluate the switching activity of the on-chip and off-chip buses at the system-level. The innovative contribution of this research is related to its capability to evaluate the effects of encoding schemes on the power consumption of system-level buses in the presence of multi-level cache memories. At that time, the research on the cache modeling problem has approached the power assessment problem only recently. This work was one of the first attempts to consider the impact of both memory hierarchy and bus encoding schemes on the power dissipation due to the processor-to-memory interface in VLSI-based system.

Scientific outcome: The results of my research have been published in [J21], [J20], [CH13], [C62], [C60], [C59], [C54], [C53], [C52], [C51]. The paper [J20] has currently a high citations count (**61**) and it has been selected to be re-published as a chapter [CH13] of the volume: “*Readings in Hardware/Software Co-design*”, Morgan Kaufmann Ed., 2001.

1.1.2. High-Level Power Optimisation

The second part of my Ph.D. thesis work focused on the definition of power minimization techniques operating at the system-level. Two main goals have been pursued: (1) the definition of bus encoding schemes for the processor-to-memory communication, and (2) the definition of state assignment algorithms for Finite State Machines.

1. My Ph.D. thesis research represents one of the first efforts to study the problem of power dissipation related to the processor-to-memory communication on the system buses. Low-power bus encoding techniques have been proposed to reduce the switching power consumption for address buses by exploiting spatio-temporal

correlations. The proposed techniques focus on address buses, which can be organized as separated or shared buses for instructions and data streams. Our approach relies on the fact that the addresses generated by a microprocessor are often consecutive, due to the spatial locality principle. The basic idea of the proposed class of codes for address buses is to avoid the transfer of consecutive addresses on the bus by adding redundancy to communicate to the receiving end of the bus the information related to the address sequentiality. The Ph.D. thesis also introduces innovative mixed techniques to jointly exploit the properties of previous bus encoding schemes to further improve the power savings. The combined encoding methods are particularly suitable for system architectures where a shared bus is used to transmit both instruction and data addresses. For these buses, the accesses to instructions and data arrays mainly occur in-sequence, but unfortunately they are often interleaved on the same address bus, thus the sequentiality is destroyed. The mixed encoding schemes aim at restoring the sequentiality. Other mixed techniques have been defined for data address buses, for which data streams accessing data arrays generate in-sequence addresses, while other data accesses generate addresses randomly distributed in time. Experimental results, conducted by tracing real address streams derived from commercial microprocessors executing benchmarks programs, have demonstrated the effectiveness of the proposed methods on the transition activity reduction. The design of low power encoding/decoding logic has also been carried out to demonstrate that the power savings achieved through activity reduction are not offset by the introduction of the redundant circuits.

Scientific outcome: The results of my research have been published in [C61], [C58], [C50]. The papers presented at **GLS-VLSI-97** [C61] and **DATE-98** [C58] have had a high research impact (so far they have respectively had **263** and **135** citations). They represent **my top ranked papers** based on Harzing's author impact analysis and Google Scholar. In 2008, the paper presented at **DATE-98** [C58] has been recognized as one of the most influential papers of the past ten years DATE and then selected to be re-published as a chapter of the volume: "**The Most Influential Papers of 10 Years DATE**", Lauwereins, Rudy; Madsen, Jan (Eds.), 2008, Springer Ed. For the low-power encoder/decoder architecture developed in collaboration with STMicroelectronics, I have been designated as inventor in the **US Patent Application [P3-US]** published in 2002 and in the **European Patent Application [P3-EU]** published in 2001.

2. The second topic focuses on the minimization of the power consumption in synchronous sequential circuits. The main objective is to define a theoretical framework to solve the state assignment problem for FSMs represented as state transition graphs (STGs). Heuristic solutions have been proposed for the minimization of the average transition activity on the state lines. The average switching activity of the nodes have been estimated by using transition probabilities derived by modeling the FSM as a Markov chain. The reported results have shown consistent improvements with respect to previous methods. **Scientific outcome:** The results have been presented at **ISCAS-98** [C57] and **ISCAS-2000** [C48].

1.1.3. Power Estimation and Optimization for VLIW Architectures

During my post-Ph.D. work at Politecnico di Milano, my research on power estimation and optimization has mainly been addressed to VLIW (Very Long Instruction Word) pipelined processors exploiting the parallelism at the instruction level (ILP). A VLIW processor is a (generally) pipelined processor that can execute, in each clock cycle, a set of explicitly parallel operations; this set of operations is statically schedule by the compiler to form a Very Long Instruction Word. My post-Ph.D. research activities were mainly related to the research contract: "*Power estimation methodologies for VLIW architectures*", in collaboration with the Advanced System Technology Division of **ST Microelectronics**. The research activity focused on the definition of a power estimation and optimization

methodology for VLIW architectures based on the **Lx/ST200** family of VLIW embedded processor cores (developed as a partnership between **HP Labs** and **STMicroelectronics**). The **ST200** family (including the ST210, ST220, ST231 processor cores) is used today for embedded media processing in a variety of audio, video and imaging consumer products.

During my post-Ph.D. at Politecnico di Milano, along with Prof. Mariagiovanna Sami, I co-advised Vittorio Zaccaria, a Ph.D. student at Politecnico di Milano, from 1999 until his graduation in February 2002. During this period, Vittorio Zaccaria and I started working on the **definition of an instruction-level energy model for VLIW pipelined processors** taking into account software parameters (such as instructions ordering, pipeline stall probability, instruction cache miss probability) and micro-architectural parameters (such as the energy contribution per instruction due to each pipeline stage and each functional unit). The work was the first to consider the problem of reducing the complexity of the energy model for VLIW processors by considering spatial and temporal correlations of the instructions in the trace. This work represented our first steps towards the definition of power estimation and exploration techniques integrated into a set of tools operating at the instruction level (such as Instruction Set Simulators) and they are characterized by efficiency and accuracy. The aim is the construction of an overall power estimation framework for VLIW processor architectures, from a system-level perspective, in which novel power optimization techniques can be validated. The power estimation methodology provide accurate power estimates associated with the data-path of a VLIW processor during an Instruction Set Simulation of a target application taking into consideration the energy cost obtained at the Register Transfer Level of the micro-architectural modules and considering the accesses to the register file, the pipeline stalls and the cache misses.

Scientific and industrial outcome: The results of the research have been published in the Proceedings of **CODES-2000** [C49] and **ICCAD-2000** [C47] and then extended in **IEEE Transactions on CAD** [J17] in 2002. Afterwards, the complexity of the power model has been reduced by introducing the concept of instruction clustering. This work has been presented at **DAC 2002** [C42] (citations count **52**) and then extended in [J10]. The proposed power-aware techniques have been applied to the **Lx/ST200** family of VLIW embedded processor cores (developed as a partnership between HP Labs and STMicroelectronics). The results of the application of the proposed VLIW power model to the **Lx/ST200** and the description of the integration of the model in the industrial design flow at the system level have been reported in **PATMOS 2001**[C43] and then extended in [J16]. The paper [C43] has had a high research impact with **80** citations: it represents **my third top ranked paper** based on Harzing's impact analysis and Google Scholar. The paper [C43] has also been selected to be re-published on ST Journal of System Research in 2003. Our most significant contributions on power-aware VLIW have been collected in the **scientific book**: "*Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems*" [B7] published by Kluwer Academic Publishers in 2003.

During the same period, we started working on a power-aware optimization technique addressing VLIW pipelined processors at the micro-architecture level. The basic idea consists of the definition of a register file write inhibition scheme to exploit the **forwarding** paths existing in the pipeline to avoid the power cost of writing/reading the short-lived variables to/from the register file. In many embedded applications, a significant number of variables are short-lived, that is their aliveness (from first definition to last use) spans only few instructions. Values of short-lived variables can then be accessed directly from the forwarding registers avoiding write/read to/from the register file. The decision to enable or not the write-back of results in the register file can be taken by the hardware control logic or anticipated by the compiler for a VLIW architecture, further reducing the control logic.

Scientific and industrial outcome: The proposed technique has been implemented for the **Lx/ST200** architecture in the context of the research project "*Power estimation methodologies for VLIW architectures*", in collaboration with the Advanced System Technology

Division of **ST Microelectronics**. For the proposed power-aware forwarding architecture, I have been designated as **inventor** in the **US Patent [P4-US] granted in 2005** and in the **European Patent Application [P4-EU]** published in 2002. The work has been present at **DATE 2001 [C46]** and then extended to **IEEE Trans. on VLSI Systems [J15]** in 2002.

Afterwards, power-aware design techniques have been proposed for the branch prediction phase of VLIW processors. The idea is based on exploiting the decompression buffer in the fetch phase of a VLIW processor for filtering the accesses to the branch predictor. The basic idea has then been extended by introducing some *hint* instructions from the compiler to inform the VLIW processor when the branch predictor must be activated thus reducing the power consumption. **Scientific outcome:** The results of the research have been presented at **GLS-VLSI 2003 [C38]**, **GLS-VLSI 2004 [C35]** and in [J14].

The research experience and accomplishments on power-aware computing lead to one of my primary (still on-going) research directions: design space exploration techniques for System-on-Chip architectures from a combined power/performance design perspective.

1.2. DESIGN SPACE EXPLORATION OF MULTI/MANY-CORE ARCHITECTURES

Challenges. The ever increasing complexity and integration densities of multiprocessor system-on-chip (MPSoC) architectures, significantly enlarges the design space of embedded computing systems. A wide range of design choices must be tuned from a multi-objective perspective, mainly in terms of performance and energy consumption, to find the most suitable system configuration for the target application. Given the huge design space to be analysed, the exploration of tradeoffs between multiple competing objectives cannot be anymore driven by a manual optimisation process based on the intuition and past experience of the system architect. Multi-objective exploration of the huge design space of next generation multi/many core architectures needs for Automatic Design Space Exploration techniques to systematically explore the design choices and to compare them in terms of multiple competing objectives (trade-offs analysis). Ideally, a designer would try all possible design choices and choose the most suitable according to the specific system requirements. Unfortunately, such an exhaustive approach is often unfeasible because of the large number of design choices to be simulated and analysed, in some cases showing some sophisticated effects on system properties that rarely enable to easily and accurately model the system behavior. Consequently, good search techniques are needed not only to find design alternatives that best meet system constraints and cost criteria, but also to prune the search space to crucial parameters to enable an effective and efficient design space exploration.

In the age of multi/many core architectures, system optimization and exploration definitely represent challenging research tasks. Although many point tools exist to optimize particular aspects of embedded systems, an overall design space exploration framework is needed to combine all the decisions into a global search space with a common interface to the optimization and evaluation tools. The state-of-the art lacks of a Design Space Exploration (DSE) framework to help the designer in the automatic selection of the most suitable system configuration for a certain application given a set of multiple competing objectives. Based on the idea to provide an automatic DSE framework, our research focused on the definition of an automatic multi-objective Design Space Exploration (DSE) framework to be used to tune the System-on-Chip architecture for the target application evaluating a set of metrics (e.g. energy, latency, throughput, bandwidth, QoR, etc.) for the next generation embedded multimedia platforms.

Our first phase of research on DSE started in 2001, while I was an Assistant Professor at the University of Milan. We started working on a heuristic exploration technique based on sensitivity of the optimization cost function with respect to the most relevant architecture parameters of the memory hierarchy (mainly cache size, block size and associativity) of parallel embedded systems. We assumed the parameters independence so as the cost of the design exploration phase grows

only linearly with respect to the size of the design space. The exploration strategy is based on the Energy-Delay Product (EDP) metric and the effectiveness of the proposed methodology has been proved through the optimization of the memory sub-system of two real-world embedded systems: the first one is based on a VLIW Lx/ST200 processor and the second one is based on the MicroSPARC2 superscalar processor. **Scientific outcome:** The results have been presented at **CODES-2001** [C45] and **ISCAS 2001** [C44] and then extended in the journal paper [J18].

Then, on September 2002 I moved back to Politecnico di Milano as an Associate Professor, where I continued my collaboration with Vittorio Zaccaria and started advising Gianluca Palermo, a Ph.D. student at Politecnico di Milano. During this period, we started working on heuristic techniques for the multi-objective design space exploration to find a good approximation of the Pareto optimal configurations. **Scientific outcome:** The results of this phase of research have been published in the Proceedings of **DATE2003** [C41], **SAC 2003**[C40], **GLS-VLSI'03** [C39] and **PATMOS'3** [C37].

Another facet of the research was focused on the definition of a methodology related to the **multi-objective co-exploration** of source code transformations and the architecture design space parameters. **Scientific outcome:** The research results have been published in collaboration with Giovanni Agosta and Gianluca Palermo in **SAC'04** [C36] and then extended in the journal paper [J9].

At that time, I also started working, along with Prof. Donatella Sciuto, to co-advising Giovanni Beltrame, a Ph.D. student at Politecnico di Milano, until his graduation in February 2006. During this period, we worked on the modeling, simulating, analysis and optimization of Multi-Processor System-on-Chip platforms. The platform has been configured to simulate and IPv4 forwarder (developed at STMicroelectronics Research Labs, Ottawa), and MPEG4 VGA encoder, and an Ogg-Vorbis encoder. These three applications have been explored and optimized in terms of both power and performance. **Scientific outcome:** The outcomes of this research have been published in the Proceedings of **CASES 2004** [C33], **DATE 2006** [C32] (then extended in the **IEEE Transactions on CAD** [J7]), **IFIP-VLSI-SOC2006** [C29] and **CODES-ISSS'06** [C28].

From January 2008, my research activity efforts were mainly dedicated to the coordination of the **FP7-MULTICUBE** European research project on "*Multi-objective Design Space Exploration of MultiProcessor-SoC Architectures for Embedded Multimedia Applications*". The project aimed at increasing the competitiveness of European industries by optimizing the design of embedded computing systems while reducing design time and costs. The primary goal of the project is to define an automatic multi-objective DSE framework to be used at design-time to find the best power/performance trade-offs while meeting system-level constraints and speeding up the exploration process. A set of heuristic optimization algorithms have been defined to reduce the exploration time, while a set of response surface modeling techniques have been defined to further speed up the process. Based on the results of the **design-time** multi-objective exploration, the MULTICUBE project also defined a methodology to be used at **run-time** to optimize the allocation and scheduling of different application tasks. The design exploration flow results in a Pareto-optimal set of design alternatives in terms of power/performance trade-offs. This set of operating points can then be used at run-time to decide how the system resources should be distributed over different tasks running on the multiprocessor system on chip.

The MULTICUBE DSE framework leverages a set of open-source and proprietary tools for the exploration, modeling and simulation to guarantee a wide exploitation of the project results in the embedded system design community. The integration of different tools is ensured by a common XML-based tool interface specification, defined to enable the independent development of modules and a seamless integration of the design tools and the data structures into a common design environment. Several industrial use cases (defined as combination of application and related architecture) have been used to assess the capabilities of the MULTICUBE design flow and tools in an industrial design process. **The MULTICUBE project has been strongly industry-driven:** industrial partners (STMicroelectronics and DS2) as well IMEC research center have defined the design techniques and tools requirements and then validated them to design some industrial use cases. The benefits of the introduction of the automatic DSE in the design

phase of embedded computing systems, justifying its introduction in industrial design processes, have been assessed in MULTICUBE project through a procedure to assess the final objective design quality and the reduction of design turnaround time by introducing such a technology on the entire design process. The benefits on the design process can be measurable and tangible like the reduction of the overall design process lead time, and qualitative or intangible like the streamlining and the reduction of human error prone repetitive operations. The DSE assessment procedure was the basis for the validation of the industrial use cases and demonstrators of the project. Validation results have been assessed based on a set of common assessment criteria on industrial case studies provided by STMicroelectronics, DS2 and IMEC. We believe that MULTICUBE research influenced the computing industry by highlighting the crucial importance of architectural DSE to automatically find power/performance tradeoffs.

In the context of the MULTICUBE project, I was leading a research group at Politecnico di Milano working on the development of **an open-source tool (MULTICUBE Explorer)** to enable an automatic and fast optimization of configurable system architectures towards a set of objective functions such as energy and delay. MULTICUBE Explorer provides a set of innovative sampling and optimization techniques to help finding the multi-objective Pareto points. It also provides an open XML interface for supporting exploration of new platforms/architectures by interacting with a system-level simulator. The MULTICUBE Explorer tool development team was lead by Vittorio Zaccaria and composed of Gianluca Palermo, Giovanni Mariani and Fabrizio Castro. The MULTICUBE Explorer open-source website has attracted a significant number of visits (**1870**) and tool downloads (**465**) from the beginning to the end of the MULTICUBE project.

Several **optimization algorithms** have been developed and then implemented in the MULTICUBE Explorer tool. The research focus is posed on new algorithms and on “ad hoc” modifications implemented in existing techniques to face with discrete and categorical variables, which are the most relevant ones when dealing with embedded systems design. The main contribution in the research field of optimization techniques for embedded systems design is indeed the high level of the obtained compromise between specialization of the algorithms and concrete usability of the DSE tools.

A typical design space exploration flow involves an event-based simulator in the loop, often leading to an actual evaluation time that can exceed practical limits for realistic applications. Chip multi-processor architectures further exacerbate this problem given that the actual simulation speed decreases by increasing the number of cores of the chip. Traditional design space exploration lacks of efficient techniques that reduce the number of architectural alternatives to be analyzed. In the proposed approach, we introduced in MULTICUBE Explorer a set of **Response Surface Modeling (RSM) techniques** to predict system level metrics by using closed-form analytical expressions instead of lengthy simulations. The principle of RSM is to exploit a set of simulations generated by one or more Design of Experiments strategies to build a surrogate model to predict the system-level metrics. The response model has the same input and output features of the original simulation based model but offers significant speed-up by leveraging analytical, closed-form functions which are tuned during a model training phase.

Scientific outcome: The results of the research carried out at Politecnico di Milano in collaboration with Gianluca Palermo and Vittorio Zaccaria appeared in **SASP2008** [C21], **SAMOS2008** [C20], **DSD2008** [C18] and **IFIP-VLSI-SOC 2008** [C17]. Then, the concept of variability-aware robustness of multi-objective optimization has then been addressed in the works presented at **ESTIMedia 2008** [C15] and **ASP-DAC 2009** [C13], while an extended version has been accepted to appear in [J2]. DSE based on multi-level modeling techniques have been investigated in **IC-SAMOS2009** [C11].

We continued to investigate about design space exploration challenges in a series of papers that make up the core of Giovanni Mariani’s Ph.D. thesis at University of Lugano. The first part of his thesis investigates design-time exploration based on optimization algorithms and Response Surface Modeling techniques. The first optimization approach proposed in the thesis work consists of a traditional multi-objective genetic algorithm (NSGA-II) which has been speeded up

by approximating some design points using an RSM based on Artificial Neural Networks (ANNs). Results have been presented at **DSD'09** [C9]. To avoid the exploration process finding solutions optimal for the approximate ANN model but sub-optimal for the real system, at every generation of the genetic algorithm some candidate configurations are simulated. The proposed optimization process adopts a statistical technique to select the candidate solutions that should be simulated and those to remain approximated. The statistical technique takes into account the model uncertainty and thus it is able to adapt its decision to the quality of the ANN model.

The second optimization approach proposed in Giovanni's thesis is an iterative design space exploration methodology exploiting the statistical properties of known system configurations to infer, by means of a correlation-based analysis, the next design points to be analyzed with low-level simulations. Results have been presented at **DAC-47** Conference in 2010 [C5] and an extended version has been accepted to appear in **IEEE Transactions on CAD** [J1]. In particular, the correlation-based RSM adopts a sound statistical method for modeling the output of computer simulations, enabling the estimation of model uncertainty in the different design regions. In this context, at each iteration, the optimization process investigates the correlation-based RSM looking for the candidate configuration which maximizes the probability of obtaining an effective improvement with respect to the configurations already simulated in the previous iterations. When a design point is characterized by a high model uncertainty, the probability of obtaining an effective improvement might increase and this mechanism forces the proposed heuristic to escape from local optima.

The second part of Giovanni's thesis addresses **the run-time management of system resources**. Running multiple applications optimally in terms of Quality of Service (e.g., performance and power consumption) on embedded multi-core platforms is a huge challenge. Moreover, current applications exhibit unpredictable changes of the environment and workload conditions which makes the task of running them optimally even more difficult. Our research presents an automated tool flow which tackles this challenge by a two-step approach: first at design-time, a Design Space Exploration (DSE) tool is coupled with a platform simulator(s) to get optimum operating points for the set of target applications. Secondly, at run-time, a lightweight Run-time Resource Manager (RRM) leverages the design-time DSE results for deciding an operating configuration to be loaded at run-time for each application. This decision is taken dynamically, by considering the available platform resources and the QoS requirements of the specific use-case. In particular, two run-time optimization scenarios have been investigated:

1. **Performance Optimization under Power Constraints.** This first scenario concerns the management of a multi-programmed embedded system **SASP2009** [C10]. In particular the problem is the partitioning of the system resources among different active applications with the goal of maximizing the overall platform performance for a given power budget constraint. In this work my main contributions are: first a design-time performance analysis based on queuing networks which enable an analytical evaluation of different operating configurations and, second, the definition of a lightweight RRM methodology able to exploit the queuing model in order to identify a suitable operating point to be set. Results have recently been published in Proceedings of **SASP 2011** [C3].
2. **Quality of Service Aware Run-time Resource Management.** This second scenario concerns the management of system resources for a multiple-stream MPEG4 encoding chip dedicated to automotive cognitive safety tasks. In particular the problem consists of the minimization of the power consumption for the given frame rate requirements on the multiple streams. Results have been presented at **DATE 2010** [C6] and then extended to [J4].

Research on design space exploration and run-time resource management techniques are still ongoing under my scientific coordination in the context of the **FP7-2PARMA** European project, mainly focusing on the **STMicroelectronics P2012** many-core computing fabric.

1.3. NETWORK-ON-CHIP ARCHITECTURES

Challenges. Given the increasing complexity of Multiprocessor System-on-Chip (MPSoC) designs, the current trends on on-chip communication architectures are converging towards the Network-on-Chip (NoC). The NoC-based design approach represents a high bandwidth and low energy solution. Using the NoC-based design approach has several other advantages, such as

scalability, reliability, IP reusability and separation of IP design from on-chip communication design and interfacing. NoC design represents a new paradigm to design MPSoC shifting the design methodologies from computation-based to communication-based.

Given these premises, during the last decade, we assisted to an increasing research effort on NoC architectures and related design methodologies. Many key design challenges of NoC have been investigated in the past years. These challenges have recently been classified in three main categories: the design of the communication infrastructure, the selection of the communication paradigm and the application mapping optimization. First, the problem of designing the communication infrastructure consists in turn of the following problems: network topology synthesis, the selection of the channel width, the buffer sizing problem and the NoC floorplanning problem. Second, the selection of the communication paradigm includes the routing problem and the choice of switching techniques (store-and-forward, cut-through, wormhole, etc) to be used. Third, the application mapping optimization problem consists in turn of the IP mapping and the task scheduling problems of an application onto the NoC platform. All these optimisation techniques should take into consideration several metrics of interest to be traded off. These metrics are mainly performance, energy, Quality of Service, reliability and security.

In this scenario, even some semi-conductor industries have started to propose some NoC-based designs. Among them, we can cite the Aetheral NoC from NXP-Philips, the STNoC from STMicroelectronics and the 80-core NoC from Intel. Several industrial design flows supporting NoC design have also been proposed, such as the CHAIN works tool suite by Silistix, the NoCexplorer and NoCcompiler frameworks by Arteris and the iNOCs tools from iNoCs. The interest demonstrated by several industries and EDA providers contributed to confirm NoC as a feasible and efficient approach to interconnect a scalable number of IP cores on a single die.

Although many scientific books and journal papers have recently been published, many challenging topics related to NoC research are still open. Power-aware design techniques at several abstraction levels represent the enabling keys for an energy-efficient design of on-chip interconnection network. In recent years, both Networks-on-Chip, as an architectural solution for high speed interconnect, and power consumption, as a key design constraint, have continued to gain interest in the design and research communities, since power and energy issues still represent one of the limiting factors in integrating multi- and many-cores on a single chip.

To address these NoC research challenges, my research is focusing on the topic of **low-power NoC for embedded architectures**, covering power and energy aware design and techniques from several perspectives and abstraction levels. More in detail, I was designated as **Principal investigator** in the 2-year research contract: "*Low Power Network on Chip and Embedded Architectures*"(2003-2005) between Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics (Agrate B.)**. The research has then been continued in the 2-year research contract: "*Low Power Network on Chip and Multiprocessor Platforms*" (2006-2008).

In 2003, I started advising Gianluca Palermo, Ph.D. student at Politecnico di Milano focusing his research work on Network-on-Chip architectures and design methodologies. We started working on a modular and flexible framework for power/performance exploration of Network-on-Chip architectures. The framework, namely **PIRATE**, has been developed as an open-source modeling, simulation and exploration framework to be used in our research development. PIRATE has first been presented at **PATMOS 2004** [C34]. Then, we setup a team composed of Matteo Monchiero and Oreste Villa, Ph.D. students at Politecnico di Milano, to start working on a structural modeling and simulation framework (namely GRAPES) for Multi-Processor System-on-Chip architectures based on Network-on-Chip. **GRAPES** [C19] is an open-source project that has been the basis for the design space exploration of NoC-based architectures.

GRAPES and PIRATE tools have been used for the exploration of distributed shared memory architectures based on NoC and an on-chip HW Memory Management Unit to dynamically manage data allocation/deallocation on the physically distributed shared memory space. The on-chip HW MMU makes the memory utilization more efficient especially for embedded

applications whose memory requirements can significantly change at run-time. For the proposed target many-core architecture, we explored different on-chip network topologies and a variable number of distributed shared memory modules. The exploration of NoC topologies can identify energy/delay tradeoffs and communication bottlenecks. Preliminary results are reported in **IC-SAMOS-VI** Conference in 2006 and then extended on the journal paper [J8].

One of the most significant results of the research team I was leading at that time at Politecnico di Milano (and composed of Matteo Monchiero, Gianluca Palermo and Oreste Villa) was on optimized *synchronization techniques* for shared memory multi-core architectures based on Network-on-Chip. Synchronization is an important concern in network-based systems, because of the relatively large latency featured by these systems, which on the other hand provides high bandwidth required by many modern multimedia applications. The proposed solution is based on the idea of locally performing synchronization operations requiring continuous polling of a shared variable, thus featuring large contentions (e.g. spin locks and barriers). A hardware module, the Synchronization Buffer (SB), is introduced to queue and to manage the requests issued by the processors. By using this mechanism, the SB provides a spin lock implementation requiring a constant number of network transactions and memory accesses per lock acquisition. The SB also supports an efficient implementation of barriers. Two different architectures (with local caches or local memories) have been explored to prove that the proposed approach is effective independently from caches and coherence schemes adopted. This work appeared in **DATE 2006** [C31], in [J12] and then published in **IEEE Transactions on VLSI Systems** in 2006 [J11]. The research work has then been continued to investigate about the efficiency and scalability of barrier synchronization on NoC-based many-core architectures. A conference paper summarizing this work appeared in **CASES** in 2008 [C16].

From 2005 to 2008, I also collaborated with ALaRI-Advanced Learning and Research Institute, part of the Faculty of Informatics of the University of Lugano (CH) to the research and management activities of the European Research Project **MEDEA+ LoMoSA+ (2A708): "Low-power expertise for Mobile & multi-media System Applications"**. My research activity on low-power Network-on-Chip architectures has been done in collaboration with **NXP Semiconductors (NL)** and **STMicroelectronics (Grenoble, F)**. The research activity carried out in LOMOSA+ project in collaboration with STMicroelectronics has been published in several papers appeared in **ASAP'07** [C27], **DSD'07** [C25] and **NanoNets'07** [C23]. These papers are mainly addressing the problems of the **application mapping optimization and topology customization for STNoC**.

At that time, I started working, along with Prof. Mariagiovanna Sami, to co-advising Leandro Fiorin, a Ph.D. student at University of Lugano focusing his research on high level services for Networks-on-Chip architectures. In his Ph.D. thesis work, the idea of adding high level services on top of the standard communication services usually provided by an interconnection network is introduced. Being the communication subsystem a central component in such a type of architecture, it can be used as an element to observe and control the global system activity in a way transparent to processing and storage cores, as well as to provide services that can be executed in parallel to protocol translation and data transmission. Three types of services have been addressed and discussed: security, run-time monitoring, and faults detection and fault tolerance.

More in detail, we started investigating about security aspects in NoCs in 2007 [C26]. In the context of NoC-based multiprocessor systems, we focus on the topic, not yet thoroughly faced, of data protection. The most relevant research result has been a data protection unit for NoC-based architectures presented in **CODES-ISSS'07** [C24] and then published in **IEEE Transactions on Computers** [J6] in 2008. We propose a secure NoC architecture composed of a set of Data Protection Units (DPUs) implemented within the Network Interfaces (NIs). The run-time configuration of the programmable part of the DPUs is managed by a central unit, the Network Security Manager (NSM). The DPU, similar to a firewall, can check and limit the access rights (none, read, write, or both) of processors accessing data and instructions in a shared memory - in particular distinguishing between the operating roles (supervisor/user and

secure/unsecure) of the processing elements. We explore different alternative implementations for the DPU and demonstrate how this unit does not affect the network latency if the memory request has the appropriate rights. We also focus on the dynamic updating of the DPUs to support their utilization in dynamic environments, and on the utilization of authentication techniques to increase the level of security.

A secure monitoring service for NoCs has been presented in **CODES-ISSS'08** [C14]. In this work, we detail for the first time a security monitoring system for NoC based architectures. Aim of the proposed system is to detect security violations in the device and to help counteract them by monitoring accesses to specific addresses in memory-mapped systems and deviations from expected NoC and system behaviours. While monitoring of NoCs has been proposed for debugging and optimal resources utilization, in our work, we discuss the basic blocks composing a security monitoring system. We detail overhead associated with their implementation, and types of attacks detected by the system. Probes, collecting information about the NoC traffic, are implemented inside OCP/IP compliant Network Interfaces (NIs). In fact, NIs represent the ideal position where performing analysis of incoming traffic and discard malicious requests. A central unit is in charge of collecting security alerts and deciding appropriate counter measures. The work on the programmable data protection device and secure programming manager system has been the subject of the **European Patent Application [P5-EU]** in 2007, afterwards extended to an Application to the USA Dept. of Commerce, Patent and trademark Office **[P5-US]** in 2008.

Run-time monitoring through NoC have then been published in **DATE 2009** [C12] and more recently in **NoCArc 2010** [C4]. We propose the idea of monitoring run-time system activities in adaptive NoC-based MPSoC platforms through the observation of transactions performed on the communication subsystem. As central element of architectures based on the communication-centric paradigm, NoCs are the ideal mean to collect information about cores, and more general system behavior. In particular, probes collecting information about system activity are implemented within OCP/IP compliant Network Interfaces (NIs). A central unit is in charge of collecting run-time information and adopting the suitable strategy for optimizing the use of system resources. Probes, working in parallel with protocol translation, do not influence core operations, and a relatively small overhead is paid in term of area consumed by the monitoring system, as well as in the amount of data transmitted by probes to the central unit. Research on run-time monitoring through NoC are still **on-going** under my scientific coordination at Politecnico di Milano in collaboration with ALaRI group based at University of Lugano.

More recently, we collaborated on NoC research topics with some visiting Ph. D. students from Universidade Federal do Rio Grande do Sul, Porto Alegre (Brasil). On-going joint research is focused on floorplanning-aware exploration for application-specific NoC [C1] and on a two-level adaptive buffer for a virtual channel router in NoCs [C2].

1.4. FAULT DETECTION AND FAULT TOLERANT CODING TECHNIQUES

The research faces the problems related to the fault detection and fault tolerance in computer systems. Two main areas of research have been addressed: the design of error correction and detection codes for computer memory sub-systems and the definition of detection codes for all unidirectional errors.

1.4.1. Error Detection and Correction Codes for Computer Memory Systems

A new class of error detection and correction codes to improve system reliability and data integrity for computer memory sub-systems has been developed. Most of computer systems adopt a memory organization based on *b-bit-per-chip* (where $b \geq 2$). For these systems, a fault in a memory device can generate one error from *1-to-b-bit*, namely *byte error*. Conventional SEC (Single Error Correction) and DED (Double Error Detection) codes are not suitable enough to get a good reliability level for *b-bit-per-chip* memory organization, because multiple bit errors are not detected and corrected or can even be miscorrected, thus losing data integrity. Therefore codes have been introduced in literature with

properties of **SBD (Single Byte error Detection)**. To further increase data integrity and to reduce the frequency of not correctable errors, we introduced a new class of codes with the following properties: SEC (Single Error Correction), DED (Double Error Detection), SBD (Single Byte error Detection) and correction of an odd number of errors per byte. This latter property increases the reliability level of the memory sub-system with respect to conventional SEC-DED-SBD codes by granting the corrections of at least the 50% of possible multiple errors in the single byte. The advantages and the redundancy introduced by the proposed class of codes have been compared to the codes in literature. The proposed class of codes are systematic, thus enabling the concurrent execution of the encoding/decoding phase e the data elaboration phase, and modular, thus simplifying the design phase and reducing area and delay.

Scientific and industrial outcome: The new class of codes has been first published in [C64] and then extended in [J22]. Afterwards, a set of automatic tools has been developed to support the automatic generation of error control codes for computer memory sub-systems starting from high-level system specification. The framework to support the automatic generation of error control codes has been published in [C63] and then extended in [J19]. For the new class of codes, I have been designated as **inventor** in both the **European Patents** [P2-EU], [P2-DE] and in the **US Patent** [P2-US]. An implementation of the new error detection and correction codes has been commercially adopted as part of the PowerScale architecture for the **Bull Escala** and **IBM RS6000** multiprocessor systems.

1.4.2. Systematic All Unidirectional Error Detection Codes for Self-Checking Architectures

A new class of systematic codes has been defined for the detection of unidirectional errors AUED (All Unidirectional Error Detection) for VLSI architectures with self-checking properties. The main results of the research (carried out as minor research theme during my Ph.D.) have been published in Proceedings of **DFT'98** [C55].

1.5. RESEARCH APPROACH

My research focused on the above described research challenges across a range of computing application domains, spanning from embedded devices to high-performance systems. My research addressed these challenges through both hardware and software design approaches to better exploit their synergy. Although my research activity has been primarily focused in the area of **computer architectures**, it required an in-depth understanding of problems related to the design of VLSI (Very Large Scale Integration) circuits and digital systems. At the same time, many of the solutions to the research problems heavily depend on application parameters and leveraging control mechanisms only possible through runtime system software. Thus, my research efforts have been cross-disciplinary.

In the above described research areas, that are tightly connected to meet power/performance tradeoffs in complex digital systems, the main exploration techniques enabled the definition of techniques and tools at different levels of abstractions. The phases of methodology definition, design and implementation can be considered tightly connected to meet a good trade-off between the different performance goals, with respect to the design constraints. During the research, the effort has been devoted to the applicability of the proposed techniques to provide CAD tools to optimize the design and verification phases of high-performance digital systems with particular emphasis on high-level design techniques. Furthermore, during the research work, a substantial effort has been devoted to demonstrate the effectiveness of the proposed methodologies through their implementation and application to industrial case studies and standard benchmarks.

1.6. RESEARCH COLLABORATIONS

My research activities have been carried out in collaboration with several national and international universities (Università degli Studi di Bologna, Politecnico di Torino, Stanford

University, Università della Svizzera Italiana, University of Cantabria, Universitat Politècnica de Catalunya, Technical University of Delft, Universidade Federal do Rio Grande do Sul), research centers (CEFRIEL (I), ALaRI - Advanced Learning and Research Institute (CH), IMEC (BE), Pacific Northwest National Laboratory (USA)) and information technologies and semiconductor companies (Group Bull, IBM, STMicroelectronics, Hewlett-Packard, Intel, Siemens Mobile Communications).

In particular, from 1996 up to now, I carried out and coordinated several research activities in collaboration with STMicroelectronics - Advanced System Technology Division. Among these collaborations, we can mention the collaborations with the groups of Research and Innovation of STMicroelectronics in Agrate Brianza (Italy) and Grenoble (F), and previously collaborations with the groups in San Diego (US), Ottawa (CA) and Manno (CH).

2. ON-GOING RESEARCH DIRECTIONS

Although many research papers have recently been published, many challenging and relevant research topics related to the area of **multi/many core architectures design** are still open. I believe there is still significant research to be done, and these research challenges will increase in importance as we scale down process technologies in the nanoscale era. Technology driven considerations (such as ultra-low-power design, resiliency, process variability) will further increase their importance on architectural design in the next coming years. There are several technology innovations (such as bundled carbon nanotubes, nanophotonics on-chip interconnect, phase-change memories, etc.) that will drive new System-on-chip research directions.

In the age of multi/many core architectures, **system design optimization and exploration** still represent a challenging task in the design and research communities. **Networks-on-Chip**, as an architectural solution for scalable high speed interconnect, and **power-aware design** will continue to represent crucial research topics to be addressed, since power and energy issues still represent one of the limiting factors in integrating multi- and many-cores on a single chip.

My on-going research activities are focused on the following research directions:

1. **Efficient strategies for automatic design space exploration.** For modern computing systems based on multi-many-core architectures, the architecture design space is huge and the evaluation of a single design point takes a lot of time because it requires the simulation of the target application on the given system. Since the overall design space is now so huge, improved heuristics are needed to prune the design space in search for tradeoff solutions. The challenge is to define efficient search strategies from a multi-objective perspective in combinatorial optimization spaces and Response Surface Modeling techniques to analytically model the system behavior.
2. **Efficient design space exploration during high level synthesis exploiting response surface methods.** In this work, we introduce a new DSE direction during HLS by investigating the usage of Response Surface Methods to analytically model an HLS engine. We propose the construction of delay and area RSM models to capture the behavior of the core HLS optimization algorithms (operation scheduling, resource binding and register allocation), enabling prediction of the design metrics for various data-path configurations resulting from the HLS phase. By adopting the proposed approach, we manage both *(i)* to eliminate the iterative resorting to the costly architectural synthesis procedures, thus accelerating exploration and *(ii)* to explore the HLS design space in a global manner. Recently, RSMs have been used in the field of platform based design to model processor architectures for reducing simulation time. Within this research work, we differentiate from the aforementioned approaches, since we are applying RSM to model and predict the behavior of HLS optimization algorithms rather than a specific processor architecture.
3. **Adaptive design and monitoring of applications for multi/many-core architectures.** Running multiple applications optimally in terms of Quality of Service (e.g., performance and power consumption) on embedded multi/multi-core platforms is a huge challenge. Moreover, current applications exhibit unpredictable changes of the environment and workload conditions which makes the task of running them optimally even more difficult. Our research proposes an approach where applications include service routines to dynamically monitor the usage of system resources in multi/many-core architectures. This information is sent to a lightweight Run-time Resource Manager (RRM) leveraging these results for deciding an operating configuration of the application parameters to be loaded at run-time for each application. This decision is taken dynamically, by considering the available platform resources and the QoS requirements of the specific application.
4. **High-level services for Network-on-Chip architectures.** In this work we plan to

monitor run-time system activities in adaptive NoC-based multi/many-core platforms through the observation of transactions performed on the communication subsystem. As central element of architectures based on the communication-centric paradigm, NoCs are the ideal mean to collect information about cores, and more general system behavior. Being the NoC the central component in multi/many architectures, it can be used as an element to observe and control the global system activity in a way transparent to processing and storage cores, as well as to provide high-level services that can be executed in parallel to protocol translation and data transmission. Three types of services have been addressed and discussed: security, run-time monitoring, and fault detection and fault tolerance.

5. **Floorplanning-aware hierarchical adaptive NoC architectures.** In this research, we focus on floorplanning-aware exploration for application-specific hierarchical NoCs. In this paper, we propose HASIN – Hierarchical Adaptive Switching Interconnection Network, an architecture that explores the suitable switching architecture according to the bandwidth requirements for each region of a system, in a hierarchical manner. The proposed interconnection allows adapting the network at runtime using three switching possibilities and for this, it uses floorplan information to reconfigure itself. The adaptability at the system level is required due to some unforeseen situations at design time. In these cases, we can consider the possibility of updates in the system with changes in the communications rates, the fact that the traffic does not present a constant behavior, as the occurrence of burst or still the reason that is not possible to integrate all cores with high communication in the same cluster due the restrictions of the crossbar size.

3. LIST OF PATENTS

	Publication number	Publication date	Inventor(s)	Applicant(s)	Application number and date
P1-EU	Integrated CMOS static RAM.				
	EP0578900 (A1)	19/01/1994	SADA GIANCARLO [IT] SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	EP19920830383 - 16/07/1992
	EU Patent Granted EP0578900 (B1)	05/11/1997			
P1-DE	Integrierter CMOS-statischer RAM.				
	DE Patent Granted DE69223046 (T2)	26/02/1998	SADA GIANCARLO [IT] SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	DE19926023046T -16/07/1992
P2-US	Digital information error correcting apparatus for single error correcting (SEC), double error detecting (DED), single byte error detecting (SBED), and odd numbered single byte error correcting (OSBEC)				
	US Patent Granted US5535227 (A)	09/07/1996	SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	US19940248140 - 23/05/1994
P2-EU	Digital information error correcting apparatus for correcting single errors (SEC), detecting double errors (DED) and single byte multiple errors (SBD), and the correction of an odd number of single byte errors (ODD SBC).				
	EP0629051 (A1)	14/12/1994	SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	EP19930830254 10/06/1993
	EU Patent Granted EP0629051 (B1)	01/04/1998			
P2-DE	Digital information error correcting apparatus for correcting single errors (SEC), detecting double errors (DED) and single byte multiple errors (SBD), and the correction of an odd number of single byte errors (ODD SBC).				
	DE Patent Granted DE69317766 (T2)	30/07/1998	SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	DE19936017766T - 10/06/1993
P3-US	Encoder/decoder architecture and related processing system				
	US2002019896 (A1)	14/02/2002	FORNACIARI WILLIAM [IT] SCIUTO DONATELLA [IT] SILVANO CRISTINA [IT] ZAFALON ROBERTO [IT] PAU DANILLO [IT]	ST MICRO-ELECTRONICS SRL [IT]	US20010843533 - 25/04/2001
P3-EU	Encoder architecture for parallel busses				
	EP1150467 (A1)	31/10/2001	FORNACIARI WILLIAM [IT] SCIUTO DONATELLA [IT] SILVANO CRISTINA [IT] ZAFALON ROBERTO [IT] PAU DANILLO [IT]	ST MICRO-ELECTRONICS SRL [IT]	EP20000830322 28/04/2000

P4-US Processor architecture					
US2002124155 (A1)	05/09/2002	SAMI MARIAGIOVANNA [IT]	ST MICRO- ELECTRONICS SRL [IT]	US20010976241 11/10/2001	
		SCIUTO DONATELLA [IT]			
		SILVANO CRISTINA [IT]			
		ZACCARIA VITTORIO [IT]			
		PAU DANILO [IT]			
		ZAFALON ROBERTO [IT]			
US Patent Granted US6889317 (B2)	03/05/2005				
P4-EU Processor architecture with variable-stage pipeline					
EP1199629 (A1)	24/04/2002	SAMI MARIAGIOVANNA [IT]	ST MICRO- ELECTRONICS SRL [IT]	EP20000830673 - 17/10/2000	
		SCIUTO DONATELLA [IT]			
		SILVANO CRISTINA [IT]			
		ZACCARIA VITTORIO [IT]			
		PAU DANILO [IT]			
		ZAFALON ROBERTO [IT]			
P5-US PROGRAMMABLE DATA PROTECTION DEVICE, SECURE PROGRAMMING MANAGER SYSTEM AND PROCESS FOR CONTROLLING ACCESS TO AN INTERCONNECT NETWORK FOR AN INTEGRATED CIRCUIT					
US2009089861 (A1)	02/04/2009	CATALANO VALERIO [FR]	ST MICRO- ELECTRONICS GRENOBLE SA [FR]	US20080207131 - 09/09/2008	
		COPPOLA MARCELLO [FR]			
		LOCATELLI RICCARDO [FR]			
		SILVANO CRISTINA [IT]			
		PALERMO GIANLUCA [IT]			
		FIORIN LEANDRO [CH]			
P5-EU Programmable data protection device, secure programming manager system and process for controlling access to an interconnect network for an integrated circuit.					
EP2043324 (A1)	01/04/2009	CATALANO VALERIO [FR]	ST MICRO- ELECTRONICS GRENOBLE SA [FR]	EP20070301411 - 28/09/2007	
		COPPOLA MARCELLO [FR]			
		LOCATELLI RICCARDO [FR]			
		SILVANO CRISTINA [IT]			
		PALERMO GIANLUCA [IT]			
		FIORIN LEANDRO [CH]			

4. LIST OF PUBLICATIONS

I have co-authored **22** top-ranked journal publications (including **12** IEEE/ACM Transactions) and **13** book chapters. I am co-author of **66** scientific publications on peer-reviewed international conferences (collecting one Best Paper Award and one of the most influential papers published in the Proceedings of DATE Conference in the decade 1998-2008). I am co-author of the book: "Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems", published by Kluwer Academic Publisher (2003). I am co-editor of the books: "Low-Power Networks-on-Chip", Springer (2010) and "Multi-objective design space exploration of multiprocessor SoC architectures", Springer (2011). **My Hirsch's h-index is 18; my Egghe's g-index is 36 and total number of citations is 1525.**

4.1. INTERNATIONAL JOURNALS WITH PEER REVIEW

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- [J2]. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "A Variability-Aware Robust Design Space Exploration Methodology for CMPs", **ACM Transactions on Embedded Computing Systems**. Vol. 10, Issue 4, August 2011. **Accepted for publication (Awaiting production)**.
- [J3]. Andrea Di Biagio, Giovanni Agosta, Cristina Silvano and Martino Sykora. "Architecture Optimization of Application-Specific Implicit Instructions". **ACM Transactions on Embedded Computing Systems**. Vol. 11. **Accepted for publication (Awaiting production)**.
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