

CURRICULUM VITAE - CRISTINA SILVANO



EDUCATION

- **Doctor of Philosophy (Ph. D.) in Computer Engineering**, Università degli Studi di Brescia (Italy), 1999.

- **Master of Science (Laurea) in Electrical Engineering**, Politecnico di Milano, 1987.

RESEARCH AREAS

With my research group consisting of 5 faculty members, we research topics in the areas of Computer Architecture and Electronic Design Automation, with particular emphasis on power aware computing for embedded systems, design space exploration for multi/many-core architectures, Network-on-Chip architectures and fault tolerant coding techniques.

ACADEMIC EXPERIENCE

I am an **Associate Professor (with tenure)** of Computer Engineering, School of Computer Engineering, Politecnico di Milano. I'm currently with the Department of Electronics and Computer Engineering, System Architectures Group. I annually teach basic and advanced courses on computer architectures and operating systems. I am currently **Project Coordinator** of the European Project FP7-2PARMA-248716 on "PARAllel PARadigms and Run-time MANagement techniques for Many-core Architectures" (Jan. 2010 - Dec. 2012). Previously I was **Project Coordinator** of the European Project FP7-MULTICUBE-216693 on "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (Jan. 2008 - June 2010).

INDUSTRIAL EXPERIENCE

From May 1987 to February 1996, I was with the R&D Laboratories of Group Bull (also known as Bull HN Information Systems), Pregnana Milanese (Italy). I was responsible for the logic design and verification methodology of VLSI circuits for computer systems and member of the ASIC Development and Validation Group in the R&D PowerPC Platform and Migration Department. From 1992, I was part of the Bull - IBM joint team for the design of the first multiprocessor systems based on PowerPC processor architecture. These systems have been fully designed in the Bull R&D Labs in Italy and then commercialized as Bull Escala UNIX Servers and as IBM RS/6000 Symmetric Multiprocessor Servers. These shared-memory multiprocessor systems are symmetric and scalable up to eight processors. The architecture has been designed to support the family of IBM PowerPC processors (PowerPC 601, 604 and 620).

SCIENTIFIC OUTPUT

I have co-authored **22** top-ranked journal publications (including **12** IEEE/ACM Transactions) and **13** book chapters. I am co-author of **66** scientific publications on peer-reviewed international conferences (collecting one Best Paper Award and one of the most influential papers published in the Proceedings of DATE Conference in the decade 1998-2008). I am co-author of the book: "Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems", published by Kluwer Academic Publisher (2003) and I am co-editor of the two books: "Low-Power Networks-on-Chip", Springer (2010) and "Multi-objective design space exploration of multiprocessor SoC architectures", Springer (2011). **My Hirsch's h-index is 18; my Egghe's g-index is 36 and total number of citations is 1525.**

PATENTS

I hold one European patent granted in 1997 for an integrated static RAM, one US patent (1996) and related EU patent (1998) for a class of error correcting and detecting codes, and one US patent (2005) for a power-aware pipeline processor architecture. I am co-inventor in other two European patent applications, then extended as US patent applications.

SCIENTIFIC SERVICES

I am an active member of the computing and embedded system design community and I regularly serve in several international program committees. I have also organized **14** international conferences and workshops as Program Chair or General Chair

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1. PERSONAL DATA

Current Position:

Associate Professor (with tenure)
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Languages:

Italian: mother tongue
English: fluent
French: basic

2. CAREER

2.1. EDUCATION

- **Doctor of Philosophy (Ph. D.) in Computer Engineering, 1999, Università degli Studi di Brescia (Italy).** Ph.D. Thesis on: “Power Estimation and Optimization Methodologies for Digital Circuits and Systems”, Advisor: Prof. P. Gubian, Università degli Studi di Brescia, Co-Advisor: Prof. D. Sciuto, Politecnico di Milano.
- **Master of Science (Laurea) in Electrical Engineering, 1987, Politecnico di Milano** (Final grade 100/100). MS Thesis on: “Theoretical and numerical study of shallow waters fluidodynamic models”, Advisor: Prof. G. Prouse (Co-Advisor Prof. L. Gotusso).

2.2. ACADEMIC CAREER

- **Associate Professor (with tenure)** of Computer Engineering, School of Computer Engineering, Politecnico di Milano (Sept. 2002 – Present). I’m currently with the Department of Electronics and Computer Engineering, System Architectures Group. I annually teach basic and advanced courses on Computer Architectures and Operating Systems. My primary research interests are in the area of Computer Architectures and Electronic Design Automation, with particular emphasis on power-aware computing for embedded systems, design space exploration for multi/many-core architectures, and Network-on-Chip architectures. I am an active member of the computing and embedded system design community and I regularly serve in several international program and organization committees. So far, I have organized **14** international conferences and workshops as Program Chair or General Chair. I am currently **Project Coordinator** of the European Project FP7-2PARMA-248716 on "PARallel PARadigms and Run-time MAnagement techniques for Many-core Architectures" (Jan. 2010 - Dec. 2012). Previously, I was **Project Coordinator** of the European Project FP7-MULTICUBE-216693 on "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (Jan. 2008 - June 2010).
- **Assistant Professor** of Computer Science at Università degli Studi di Milano, School of Mathematical Physical and Natural Sciences, Department of Computer Science (October 2000 – August 2002). I annually taught basic and advanced courses on Computer Architectures and Operating Systems. My research activity focused on power-aware computing.
- **Post-Doctoral Researcher** at Politecnico di Milano, Department of Electronics and Computer Engineering (Sept. 1999 – Sept. 2000). My research activities were mainly related to the research contract: “*Power estimation methodologies for VLIW architectures*”, in collaboration with the Advanced System Technology Division of ST Microelectronics.
- **Research Staff Member**, Electronic Design Automation Area at CEFRIEL (Center for the Research and the Education in Information Engineering) in Milan (Nov. 1998 – August 1999). My research activity was mainly part of the project TOSCA (Tools for System Co-design Automation) and the European Project No. 26796 PEOPLE (Power Estimation for fast exPLoration of Embedded systems).
- **Research Assistant**, Università degli Studi di Brescia (Italy), Department of Computer Engineering (March 1996 – Oct. 1998). My research activity focused on power estimation and optimization methodologies for embedded systems.

2.3. INDUSTRIAL CAREER

From May 1987 to February 1996, I was with the **R&D Laboratories of Groupe Bull** (also known as Bull HN Information Systems), Pregnana Milanese (Italy):

- From May 1987 to March 1992, I held the position of **Research and Design Engineer** in the VLSI Design Group, Technology and Hardware Methodology Dept., where I worked on logic design and verification methodology of VLSI circuits for computer systems.
- From April 1993 to February 1996, I held the position of **Senior Research and Design Engineer** in the ASIC Development and Validation Group, R&D PowerPC Platform and Migration Department. I participated to the design of several VLSI circuits for Groupe Bull computer systems. I have also been involved in the definition of design and simulation methodologies at the system-level.

From 1992, I was part of the **Bull - IBM joint team** for the design of the first multiprocessor systems based on PowerPC processor architecture. These systems have been fully designed in the Bull R&D Labs in Italy and then commercialized as Bull Escala UNIX Servers and as IBM RS/6000 Symmetric Multiprocessor Servers. These shared-memory multiprocessor systems are symmetric and scalable up to eight processors. The architecture has been designed to support the family of IBM PowerPC processors (PowerPC 601, 604 and 620). During my experience at Groupe Bull, I have been involved in the following activities:

- From September 1988 to October 1990, I was in the design team of a full-custom 32-bit CISC CPU including a virtual Memory Management Unit. The CPU was designed for a system based on the GCOS6 Bull proprietary OS. During the design, I worked at the **Bull R&D Labs, Billerica (MA - USA)** on November 1988 and on April-May 1989. I also worked at the VLSI design center of **VLSI Technology Inc., Munich (Germany)** from February to March 1990, and at **VLSI Technology Inc. in S. José (CA-USA)** on April 1990. For her contribution to the microprocessor design and verification, I received the **“1991 Bull Technical Award”**.
- In 1990, I designed a Dual Port SRAM module generator based on a process-independent design methodology. The generator (described in [C65]) has been used to synthesize two embedded memories integrated in a VLSI circuit designed for the European project ESPRIT2 -IDPS (Integrated Design and Production System) No. 5075 (1990-1992). In 1992, I have been designated as inventor of the hierarchical and modular memory architecture in the **European patent [P1-EU]** granted in 1997.
- From 1991 to July 1992, I was with the Bull Advanced Technology Group, responsible for the introduction of new technologies and methodologies in the design of integrated circuits for computer systems.
- From August 1992, I was part of the **Bull-IBM (Austin-US) design team** of the chip set for the Bull Escala multiprocessors, which are symmetric and scalable systems based on shared memory architecture and composed of two to eight processors. The Escala systems have been **the first worldwide multiprocessors based on the PowerPC processor architecture** (PowerPC 601, 604e e 620). **The systems have been fully developed at the R&D Bull Labs in Italy by a Bull-IBM joint team** and then commercialized as **Bull Escala UNIX Servers** and as IBM RS/6000 Symmetric Multiprocessor Servers.
- For these **Escala/RS6000 multiprocessor systems**, I was responsible for the design and simulation of a four-ASIC chip-set implementing the 64-bit data cross bar architecture, named **PowerScale**, connecting four processor nodes (including two processors each), the I/O node (including two I/O channels), and the shared memory. The PowerScale architecture has been adopted by many commercial series of the Bull Escala servers. The

chip-set includes a new error detection and correction code to improve system reliability and data integrity. From this code, I developed the construction techniques for a new class of codes for computer memory sub-systems [J22], [J19], [C63], [C64]. For the new class of codes I have been designated as **inventor** in both the **European Patents** [P2-EU], [P2-DE] and in the **US Patent** [P2-US]. Afterwards, a tool has been developed to support the automatic generation of error control codes for computer memory sub-systems starting from high-level system specification.

- From June 1993 to July 1994, I was involved in the logic and timing verification of a 120K gates ASIC with the functionality of secondary cache controller for both the PowerPC 601 and 604 processors and designed for the **Escala/RS6000 multiprocessor systems**. The ASIC implements the cache coherency mechanism both vertically (between the different cache levels of each processor) and horizontally (among different processors). The cache coherency is based on the MESI protocol.
- From September 1994 to December 1995, I was a member of the team for the design and simulation of a 230K gates ASIC with the functionality of memory controller for the **Escala/RS6000 multiprocessor systems**, based on a shared and interleaved memory sub-system. The ASIC manages also the data-cross bar architecture, PowerScale, for the new series of multiprocessor systems: Escala-E and Escala-T. More in detail, The Escala-E servers support up to two processors (PowerPC 604e or 620), the shared memory configurable from 16MB to 2 GB, and a single 64-bit PCI bus. The Escala-T servers support up to four processors (PowerPC 604e or 620), the shared memory configurable from 32 MB to 3 GB, and two 64-bit PCI buses. The architecture of the memory sub-system is completely interleaved up to the level of the cache block of 32B and it aims at minimizing the conflicts among processors for the usage of the shared memory. During this project, I have also been involved in the definition of the system-level simulation, based on VHDL models of the processors, I/Os and the whole chip-set, which includes the memory controller, the data cross-bar and the centralized arbiter of the system-bus.
- During the Academic Years 1993/94 and 1994/95, I also held the position of **Bull Senior Researcher** responsible for some Master students in Information Technology at **CEFRIEL** – Research and Training Center in Milano in the Electronic Design Automation area. The activities were partially funded by the European Project EUREKA/JESSI (Joint European Submicron Initiative) – Subprogram Application AC-5.

3. RESEARCH ACTIVITIES

My research is primarily focused on the area of **Computer Architectures** and **Computer Aided Design Methodologies**, with particular emphasis on the following four research topics:

1. *Power-Aware Computing for Embedded Systems*

The main goal of the research is to develop design techniques for the phases of analysis and synthesis of digital circuits and systems to reduce the power consumption at the higher levels of abstractions. The research activity is mainly focused on two main areas: **estimation and optimization of power dissipation**. The proposed power estimation and optimization techniques are mainly addressed to embedded computing architectures based on **VLIW (Very Long Instruction Word) pipelined processors**. The proposed techniques have been applied to the Lx/ST200 family of VLIW embedded processor cores (developed as a partnership between HP Labs and STMicroelectronics). The ST200 family (including the ST210, ST220, ST231 processor cores) is used today for embedded media processing in a variety of audio, video and imaging consumer products.

2. *Design Space Exploration of Multi/Many-Core Architectures*

The aim of the research is to investigate on power/performance tradeoffs in parallel on-chip architectures. The exploration techniques are based on **multi-objective optimization** algorithms and energy/delay estimation metrics. The basic idea is to provide an automatic DSE methodology for the analysis of system characteristics and the selection of the most appropriate architectural solution to satisfy system requirements mainly in terms of performance and power consumption. From January 2008, my research activity efforts were mainly dedicated to the coordination of the European research project, namely **MULTICUBE** standing for “*Multi-objective Design Space Exploration of MultiProcessor-SoC Architectures for Embedded Multimedia Applications*”, aimed at increasing the competitiveness of European industries by optimizing the design of embedded computing systems while reducing design time and costs. The primary goal of the project is to define an automatic multi-objective DSE framework to be used at design-time to find the best power/performance trade-offs while meeting system-level constraints and speeding up the exploration process. A set of heuristic optimization algorithms have been defined to reduce the exploration time, while a set of response surface modeling techniques have been defined to further speed up the process. Based on the results of the *design-time* multi-objective exploration, the research also defined a methodology to be used at *run-time* to optimize the allocation and scheduling of different application tasks. So far, the proposed methodology has been applied to several application domains to demonstrate their applicability and benefits in industrial contexts.

3. *Network-on-Chip Architectures*

Given the increasing complexity of Multiprocessor System-on-Chip (MPSoC) designs, the current trends on on-chip communication architectures are converging towards the Network-on-Chip (NoC) approach representing a high bandwidth and low energy solution. Using the NoC-based design approach has several other advantages, such as scalability, reliability, IP reusability and separation of IP design from on-chip communication design and interfacing. NoC design represents a new paradigm to design MPSoC shifting the design methodologies from computation-based to communication-based. To address these NoC research challenges, my research is focusing on the topic of **low-power NoC for embedded architectures**, covering power and energy aware design and techniques from several perspectives and abstraction levels. We first worked on PIRATE, a modular and flexible framework for power/performance exploration of Network-on-Chip architectures. The framework has been used have been used for the exploration of distributed shared memory architectures based on NoC. Then, **synchronization techniques** for shared memory multi-core architectures based on Network-on-Chip have been proposed. Our research is also addressing the problems of

the application mapping optimization and topology customization for the industrial STNoC architecture. Finally, we started investigating about security aspects in NoCs and adding high level services on top of the standard communication services usually provided by an interconnection network.

4. *Fault Detection and Fault Tolerant Coding Techniques*

The research faces the problems related to the fault detection and fault tolerance in computer systems. Main goals of the research are, from one side, the design of error control codes and, from the other side, the definition of detection codes for unidirectional errors. Starting from the proposed coding schemes, a set of automatic tools to support the design of the proposed coding techniques has been defined.

*More details about my research directions and my research accomplishments can be found in my **Research Statement** and my **List of Publications** and **List of Patents**.*

3.1. *COORDINATION OF EUROPEAN RESEARCH PROJECTS*

- I am currently **Project Coordinator** of the **European Project FP7-2PARMA-248716** on "PARAllel PARadigms and Run-time MAnagement techniques for Many-core Architectures" (Jan. 2010 - Dec. 2012). EC Contribution to the project: 2.74 Mio Euro. The 2PARMA Consortium is composed of seven partners: Politecnico di Milano (Italy), STMicroelectronics (Italy and France), Heinrich Hertz Institute - Fraunhofer Institute for Telecommunications (Germany), IMEC (Belgium), ICCS - Institute of Communication and Computer Systems (Greece), RWTH Aachen University (Germany), Synopsys (Belgium). The 2PARMA project focuses on the definition of a parallel programming model combining component-based and single-instruction multiple-thread approaches, run-time resource management policies and design space exploration methodologies for Many-core Computing Fabrics.
- Previously I was **Project Coordinator** of the **European Project FP7-MULTICUBE-216693** on "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (Jan. 2008 - June 2010). EC Contribution to the project: 2.098 Mio Euro. The MULTICUBE Consortium was composed of nine partners: Politecnico di Milano (Italy), Design of Systems on Silicon – DS2 (Spain), STMicroelectronics (Italy), IMEC (Belgium), ESTECO (Italy), University of Lugano - ALaRI (Switzerland), University of Cantabria (Spain), STMicroelectronics Beijing (China), Institute of Computing Technology – Chinese Academy of Sciences (China). The MULTICUBE project finished in 2010 with an *excellent evaluation* by the EC demonstrating to fully achieve its objectives and scientific/technical goals. More in detail, the project has demonstrated the benefits of using automated design exploration techniques (based on enhanced multi-objective optimization algorithms) by implementing a number of industrial use-cases; practical ways to trade off accuracy for speed through the use of multi-abstraction level simulation thus enabling exploration of larger design spaces; the feasibility of automated parameter tuning at run-time using exploration data collected at design-time. Based on the opinion of the European reviewers, the MULTICUBE project management team demonstrated high leadership capabilities and led very professionally all the management activities. In the context of the MULTICUBE project, I was also leading a research group at Politecnico di Milano whose research focuses on design space exploration for multi-processor architectures working on an open-source tool (**MULTICUBE Explorer**) to enable an automatic and fast optimization of configurable system architectures towards a set of objective functions such as energy and delay. MULTICUBE Explorer provides a set of innovative sampling and optimization techniques to help finding the multi-objective Pareto points. It also provides an open XML interface for supporting exploration of new platforms/architectures by interacting with a system-level simulator.

3.2. *PARTICIPATION TO EUROPEAN RESEARCH PROJECTS*

- I am currently participating as **WP Leader** to the **ARTEMIS SMECY** Project on "Smart Multicore Embedded Systems" (start date: 01/02/2010). The SMECY project includes 30

partners from 9 European countries (among others we can cite STMicroelectronics and Thales). Project Coordinator: Francois Pacull (CEA, France).

- I am currently participating to the **European Integrated Project COMPLEX - 247999** on "Co-design and power management in platform-based design space exploration" (Start date: 01/12/2009). EC Contribution to the project: 4.8 Mio Euro. The COMPLEX project includes 14 partners from 6 countries (including China). Project Coordinator: OFFIS – Germany. Project Partners: Thales Communications SA –France, Synopsys Belgium NV – Belgium, Universidad de Cantabria – Spain, EDALAB Srl –Italy, Magillem Design Services SAS – France, STMicroelectronics Srl – Italy, STMicroelectronics (Beijing) – China, GMV Aerospace and Defence – Spain, Politecnico di Milano – Italy, Politecnico di Torino – Italy, Chipvision Design Systems– Germany, IMEC – Belgium, ECSI – France.
- From 2005 to 2008, I collaborated with ALaRI-Advanced Learning and Research Institute, part of the Faculty of Informatics of the University of Lugano (CH) to the research and management activities of the European Research Project **MEDEA+ LoMoSA+ (2A708)**: "*Low-power expertise for Mobile & multi-media System Applications*". LoMoSA project partners come from industry (NXP, STMicroelectronics, Thales, Thomson), university research labs and institutes (CEA-LETI, CEA-LIST, TIMA, ALaRI, University of Cantabria) and there is also one SME (DS2). Our research activity on low-power Network-on-Chip architectures has mainly been done in collaboration with NXP Semiconductors (NL) and STMicroelectronics (Grenoble, F). The activity carried out in this project has been published in several papers and it has been the subject of a **patent application** to the European Patent office, afterwards extended to the USA Dept. of Commerce, Patent and trademark Office.
- From 2004 to 2007, I participated to the FP6 European STREP Project **ICODES – 004452** (Interface and communication based design of embedded systems). EC Contribution to the project: 2.850 Mio Euro. Project partners: OFFIS (D - Project Coordinator), Magillem Design Services (F), Nokia Simenes Networks (I), Robert Bosch (D), European Electronic Chips & Systems Design Initiative (F), Thales Communications (F), Politecnico di Milano (I).
- I participated to the **Integrated Action Italy-Spain 2006** (Project No. AIIS05E5AB) "HW/SW Parallelism Exploitation in Chip Multiprocessor Architectures". Italian principal investigator: prof. M. Sami – Politecnico di Milano. Spanish principal investigator: prof. Antonio Gonzalez, Universitat Politecnica de Catalunya (Barcelona).
- I participated to **European Project No. 26796 PEOPLE** (Power EstimatiOn for fast exPLoration of Embedded systems) funded by ESPRIT4-OMI (Open Microprocessor Initiative) from 1/4/1998 to 31/12/2000. Project partners: Alcatel, ARM, Italtel, LEDA (Languages for Design Automation), OFFIS-University of Oldenburg e Politecnico di Torino- CEFRIEL.

3.3. PARTICIPATION TO INDUSTRIAL FUNDED RESEARCH PROJECTS

- **Principal Investigator** in the 2-year research contract: "*Low Power Network on Chip and Multiprocessor Platforms*" (2006-2008) between the Dipartimento di Elettronica e Informazione del Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics**, Agrate B.
- **Principal Investigator** in the 2-year research contract: "*Low Power Network on Chip and Embedded Architectures*"(2003-2005) between the Dipartimento di Elettronica e Informazione del Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics**, Agrate B.
- Previously, I participated to the 2-year research contract: "*Power estimation methodologies for VLIW architectures*"(2000-2002) between the Dipartimento di Elettronica e Informazione del Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics**, Agrate B. I actively participated to the scientific research related to this project. The activity carried out in this project has been published in several

papers and it has been the subject of a **patent granted** by the European Patent office, afterwards extended to the USA Dept. of Commerce, Patent and trademark Office.

3.4. PARTICIPATION TO NATIONAL RESEARCH PROJECTS

- Two-year scientific National research project: **CNR Italian Research Council - 1997-98 Project**: “Metodologie e Strumenti per la Progettazione Automatica di Circuiti e Sistemi Digitali a Basso Consumo di Potenza”. (Methodologies and Tools for the Automatic Design of Low-Power Digital Circuits and Systems) in collaboration with: Politecnico di Torino, Politecnico di Milano, Università degli Studi di Brescia, Università degli Studi di Ferrara. Scientific Chair: Prof. M. Mezzalama, Politecnico di Torino.
- Two-year scientific national inter-university co-funded research program **MIUR –2002** (Prot. 2002092153) “Metodologie di progetto per sistemi digitali integrati su singolo chip di tipo embedded”(Design methodologies for embedded digital systems integrated on a single chip) National Scientific Coordinator: prof. M. Sami (Politecnico di Milano) in collaboration with: Politecnico di Milano, Università degli Studi di Bologna, Università degli Studi di Urbino “Carlo Bo”, Università degli Studi di Catania, Università degli Studi di Verona, Politecnico di Torino, Università degli Studi di Roma “La Sapienza”.
- Two-year scientific National inter-university co-funded research program **MIUR – PRIN 2005** (Prot. 2005095528)“Metodologie di progettazione di sistemi multiprocessore on-chip basati sul concetto di piattaforma” (Design methodologies of multiprocessor systems-on-chip based on the concept of platform) National Scientific Coordinator: prof. D. Sciuto (Politecnico di Milano) in collaboration with: Politecnico di Milano, Politecnico di Torino, Università degli Studi di Bologna, Università degli Studi di Catania, Università degli Studi di Verona.
- National scientific research project **FIRB – MAIS** – “Sistemi informativi adattativi multicanale - modelli, metodologia, piattaforma abilitante a oggetti e architetture per sistemi informativi on-line flessibili”, Scientific Coordinator: prof. B. Pernici (Politecnico di Milano) Partners: Politecnico di Milano, Università degli Studi di Roma "La Sapienza", Università degli Studi Roma Tre, Università degli Studi di Lecce, STMicroelectronics, Università degli Studi di Milano-Bicocca, CEFRIEL-Milano, Engineering Ingegneria Informatica – Roma.

4. INVITED TALKS AND SEMINARS

1. April 7th, 2011, Invited Talk: "2PARMA Project: PARallel PARadigms and Run-time Management techniques for Many-core Architectures", HIPEAC Cluster Meeting on Multi-core Architectures, 2011 Chamonix (F), Host: Per Stenström, Professor, Chalmers University of Technology, Sweden.
2. November 24th, 2010, Invited Talk: "Automatic Design Space Exploration for Chip Multi-processors", Workshop on "Challenges in Embedded System Design": Involvement of SMEs in Designing Complex Systems (CMM 2010), University of Lugano, Switzerland, Workshop Organizers: G. De Micheli (EPFL) and M. Sami (USI-Politecnico di Milano).
3. July 6th, 2010, Invited Talk: "MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures", Research Projects Workshop at ISVLSI 2010: IEEE Computer Society Annual Symposium on VLSI, July 5-7, 2010, Lixouri Kefalonia, Greece.
4. June 18th, 2010, Seminar at Department of Computer Science & Engineering, University of California, Riverside, CA, USA, "Automatic Design Space Exploration for Chip-Multi Processors" (Slides). Host: Walid Najjar, Professor, Computer Science and Engineering, University of California Riverside.
5. June 17th, 2010, Seminar at Department of Computer Science & Engineering, University of California, Irvine, CA, USA, "Automatic Design Space Exploration for Chip-Multi Processors" (Slides). Host: Alexander V. Veidenbaum, Professor, Dept. of Computer Science, University of California Irvine.
6. March 23th, 2010, Seminar at Delft Technical University, Computer Engineering Colloquium Series. Title of the seminar: "A Design Space Exploration Framework for Run-Time Resource Management on Multi-Core Architectures" (Slides). Host: Prof. Koen Bertels, Delft Technical University (NL).
7. December 17, 2009, Seminar at NEC Laboratories America, Inc., Princeton Campus, Princeton (NJ - USA), Title of the seminar: "Automatic Design Space Exploration for Chip-Multi Processors". Host: Dr. Marcello Lajolo (NEC Laboratories America).
8. December 16, 2009, Seminar at Princeton University, Department of Electrical Engineering, Computer Engineering Seminar, Title of the seminar: "Automatic Design Space Exploration for Chip-Multi Processors", Host: Prof. Ruby Lee, Princeton University.
9. July 29th, 2009, Seminar at HP Labs, Palo Alto, Title of the seminar: "MULTICUBE Explorer: Leveraging DoE/RSM-based Techniques to Automate Design Space Exploration for CMPs", Host: Dr. Matteo Monchiero (Exascale Computing Lab, HP Labs, Palo Alto).
10. May 14th, 2009, Seminar at Delft Technical University, Computer Engineering Colloquium Series. Title of the seminar: "MULTICUBE Explorer: Leveraging DoE/RSM-based Techniques to Automate Design Space Exploration for CMPs" Host: Prof. Koen Bertels, Delft Technical University (NL).
11. 25/4/2006, Seminar at Delft Technical University, Computer Engineering Colloquium Series. Title of the seminar: "Exploration and Optimization of Multiprocessor Embedded Architectures based on Networks-on-Chip", Host: Prof. Stamatis Vassiliadis, Delft Technical University (NL).
12. 22/9/2005, New York, USA, Panelist at WASP 2005 Workshop on Application Specific Processors (co-located with International Conference on Hardware/Software Codesign and System Synthesis), Panel title: "Application Specific Customizations: Processor or System Level?" Moderator: Daniel Gajski, UC Irvine.

5. SCIENTIFIC SERVICES

I'm an active member of the computing and embedded system design community, and I've organized 14 international conferences and workshops as Program Chair or General Chair and I regularly serve in several international program committees.

5.1. ORGANIZATION OF CONFERENCES AND WORKSHOPS

1. Program Co-Chair, **ASAP12**, 23rd IEEE International Conference on Application-specific Systems, Architectures and Processors, 9-11 July 2012, Delft, The Netherlands
2. Co-Organizer and General Co-Chair, **DEPCP 2012**, Fourth DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Dresden, March 16th, 2012.
3. Co-Organizer **RAPIDO Workshop 2012** on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2012, Paris.
4. Co-Organizer and General Co-Chair, **DEPCP 2011**, Third DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Grenoble, March 18th, 2011.
5. Co-Organizer **RAPIDO Workshop 2011** on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2011, Crete.
6. Program Co-Chair **ARCS 2011** - Architecture of Computing Systems Conference, Como (Italy), Feb. 2011.
7. Co-Organizer and Architectures Session Chair, **DEPCP 2010**, Second DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Dresden, March 12th, 2010.
8. Co-Organizer **RAPIDO Workshop 2010** on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2010, Pisa
9. Co-Organizer and General Co-Chair of **PARMA Workshop 2010** on Parallel Programming and Run-time Management Techniques for Many-core Architectures, co-located with ARCS 2010 - Architecture of Computing Systems Conference, Hannover (D), 2010.
10. Program Co-Chair **SASP 2010**, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference), Anaheim, CA, June 13-18, 2010.
11. Co-Organizer and Architectures Session Chair, **DEPCP 2009**, First DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Nice, April 24th, 2009.
12. General Co-Chair **SASP 2009**, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) San Francisco, CA, July 27-28, 2009.
13. Program Co-Chair **SAMOS IX Workshop** on Systems, Architectures, Modeling and Simulation, Samos, Greece, July, **2009**
14. General Co-Chair **MICRO-41**, The 41st Annual IEEE/ACM International Symposium on Microarchitecture, Como (Italy), Nov. **2008**.

5.2. MEMBER OF PROGRAM COMMITTEES

1. Program Committee Member, **DAC 2012**, ACM/IEEE Design Automation Conference, ESS6 Track Co-Chair on: "Embedded Systems Design Methodologies" San Francisco CA, 3-7 June 2012.
2. Program Committee Member, **NOCS 2012**, ACM/IEEE International Symposium on Networks-on-Chip, 2012.
3. Program Committee Member, **DATE 2012**, IEEE/ACM Design and Test in Europe Conference, Track on: "Architectural and Microarchitectural Design", 2012.
4. Program Committee Member, **HPCA-18**, The 18th International Symposium on High Performance Computer Architecture, **2012**, Feb. 25-29, 2012, New Orleans (US).
5. Program Committee Member, **ARCS 2012** - Architecture of Computing Systems Conference, 2012.
6. Program Committee Member, ACM International Conference on **Computing Frontiers 2012**.
7. Program Committee Member, **IC-SAMOS 2012**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2012.

8. Program Committee Member, **WRC 2012**, Workshop on Reconfigurable Computing, co-located with HiPEAC Conference, 2012.
9. Program Committee Member, **PDP 2012** - The 20th Euromicro International Conference on Parallel, Distributed and Network-Based Computing, 15-17 February 2012, Garching near Munich, Germany
10. Program Committee Member, **DAC 2011**, ACM/IEEE Design Automation Conference, Track ESS6 on: "Design Space Exploration and Optimization" San Diego CA, 5-10 June 2011.
11. Program Committee Member, **NOCS 2011**, ACM/IEEE International Symposium on Networks-on-Chip, 2011.
12. Program Committee Member, **DATE 2011**, IEEE/ACM Design and Test in Europe Conference, Track on: "Architectural and Microarchitectural Design", 2011.
13. Program Committee Member, **SASP 2011**, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) San Diego CA, 5-6 June 2011.
14. Program Committee Member, **ICPP2011**, International Conference on Parallel Processing, Taipei, Taiwan, Sept. 13-16, 2011.
15. Program Committee Member, **ICCD 2011**, International Conference on Computer Design, 2011.
16. Program Committee Member, **ARCS 2011** - Architecture of Computing Systems Conference, 2011.
17. Program Committee Member, **VLSI-SOC 2011**, IFIP/IEEE International Conference on very Large Scale Integration, 2011.
18. Program Committee Member, **IC-SAMOS 2011**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2011.
19. Program Committee Member, **WRC 2011**, Workshop on Reconfigurable Computing, co-located with HiPEAC Conference, 2011.
20. Program Committee Member, **MICRO-43**, The 43rd Annual IEEE/ACM International Symposium on Microarchitecture, Atlanta (US), 2010.
21. Selection Committee Member, IEEE MICRO Special Issue on **Top Picks 2010** from Computer Architecture Conferences, January/February 2011.
22. Program Committee Member, **NOCS 2010**, ACM/IEEE International Symposium on Networks-on-Chip, 2010.
23. Program Committee Member, **DATE 2010**, IEEE/ACM Design and Test in Europe Conference, Track on: "Architectural and Microarchitectural Design", 2010.
24. Program Committee Member, **ARCS 2010** - Architecture of Computing Systems Conference, 2010.
25. Program Committee Member, **HiPEAC 2010**, International Conference on High-Performance Embedded Architectures and Compilers, 2010.
26. Program Committee Member, **VLSI-SOC 2010**, IFIP/IEEE International Conference on very Large Scale Integration, 2010.
27. Program Committee Member, **IC-SAMOS 2010**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2010.
28. Program Committee Member, **WRC 2010**, Workshop on Reconfigurable Computing, co-located with HiPEAC Conference, 2010.
29. Program Committee Member, **NOCS 2009**, ACM/IEEE International Symposium on Networks-on-Chip, 2009.
30. Program Committee Member, **DATE 2009**, IEEE/ACM Design and Test in Europe Conference, Track on: "Power Estimation and Optimization ", 2009.
31. Program Committee Member, ACM International Conference on **Computing Frontiers 2009**.
32. Program Committee Member, **VLSI-SOC 2009**, IFIP/IEEE International Conference on very Large Scale Integration, 2009.
33. Program Committee Member, **IC-SAMOS 2009**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2009.
34. Program Committee Member, **DATE 2008**, IEEE/ACM Design and Test in Europe Conference, Track on: "Power Estimation and Optimization ", 2008.
35. Program Committee Member and Publicity Chair, **SASP 2008**, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) Anaheim, CA, June 8-9, 2008.

36. Program Committee Member, **VLSI-SOC 2008**, IFIP/IEEE International Conference on very Large Scale Integration, 2008.
37. Program Committee Member, **IC-SAMOS 2008**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2008.
38. Program Committee Member, **DATE 2007**, IEEE/ACM Design and Test in Europe Conference, Track on: "Power Estimation and Optimization ", 2007.
39. Program Committee Member and Publicity Chair, Workshop on Application Specific Processors (**WASP**), 2007.
40. Program Committee Member, **IC-SAMOS 2007**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2007.
41. Program Committee Member, **DATE 2006**, IEEE/ACM Design and Test in Europe Conference, Track on: "Power Estimation and Optimization ", 2006.
42. Program Committee Member, **IC-SAMOS 2006**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2006.
43. Program Committee Member, **ICS 2006**, the 20th ACM International Conference on Supercomputing, 2006.
44. Program Committee Member, **DATE 2005**, IEEE/ACM Design and Test in Europe Conference, Track on: "Power Estimation and Optimization ", 2005.
45. Program Committee Member, Workshop on Application Specific Processors (**WASP**), 2005.
46. Program Committee Member, Workshop on Application Specific Processors (**WASP**), 2004.

5.3. ASSOCIATE EDITOR AND JOURNAL REVIEWER

From 2003 to 2005 I have been *Associate Editor* of the Journal of Systems Architecture – The EUROMICRO Journal, Elsevier Ed. Since 1993 to present, I'm servicing as **reviewers** for several top ranking international journals, among them we can mention:

- IEEE Transactions on Computer
- IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems
- IEEE Transactions on Very Large Scale Integration Systems
- IEEE Design and Test
- IEEE Micro
- ACM Transactions on Design Automation of Electronic Systems
- ACM Transactions on Embedded Computing Systems
- Journal of VLSI Signal Processing Systems- Springer
- EURASIP Journal on Embedded Systems – Hindawi Publishing Corporation
- IET Computers and Digital Techniques

5.4. REVIEWER FOR VARIOUS SCIENCE FOUNDATIONS

- In 2010 and 2011, I have been called from the European Commission as **Independent Expert** to evaluate proposals submitted to the **FET-Open** programme on FP7-ICT-2009 Information and Communication Technologies.
- From November 2010, I have been called from the European Commission as Independent Expert to review the FP7 – STREP Project 248976 REFLECT (Rendering FPGAs to Multi-Core Embedded Computing) coordinated by Dr. Zlatko Petrov, Honeywell International.
- In 2010, I have been called as Reviewer of research proposals submitted to Programme Blanc International Edition 2010, ANR (Agence Nationale de la Recherche), France.
- In 2008, I have been invited as **Member of the Review Panel** for Computer Science, Academy of Finland, Research Council for Natural Sciences and Engineering. In 2009 she has been invited as **Chair** of the same review panel.
- In 2007, I have been called as **Primary Evaluator** for research projects at INRIA (French National Institute for Computer Science- France).
- From 2005 to 2008, I have been called from the European Commission as **Independent Expert** to review the Network-of-Excellence project FP6 - IST-4408 HiPEAC (High-Performance Embedded Architectures and Compilers) coordinated by prof. Mateo Valero, Universidad Politecnica de Catalunya, Barcelona.

- In April 2005, I have been called from the European Commission as **Independent Expert** to evaluate project proposals submitted to the **IV Call IST (Information Society Technology) - FP6** (6th Framework Programme) on *Nanoelectronics*.

5.5. MEMBERSHIP OF PROFESSIONAL ORGANIZATIONS

- Since 1993 I am a Member of IEEE (Institute of Electrical and Electronics Engineers).
- Since August 1999 I am a **Senior Member** of IEEE (Institute of Electrical and Electronics Engineers).
- Since 2008 I am a Member of HiPEAC Network of Excellence.

6. TEACHING ACTIVITIES

6.1. TEACHING ACTIVITY AT UNIVERSITIES

Academic Year 2011/2012

- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English)
- "Computer Architectures and Operating Systems" (10 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus

Academic Year 2010/2011

- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English)
- "Computer Architectures and Operating Systems" (10 credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus

Academic Year 2009/2010

- "Architectures for multimedia systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English)
- "Computer Architectures and Operating Systems" (10 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus

Academic Year 2008/2009

- "Architectures for multimedia systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English)
- "Hardware/software co-design methodologies" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus.

Academic Year 2007/2008

- "Architectures for multimedia systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English)
- "Hardware/software co-design methodologies" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus
- "Computer Science Fundamentals" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus

Academic Year 2006/2007

- "Architectures for multimedia systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English)
- "Hardware/software co-design methodologies" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus
- "Computer science fundamentals" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus
- "Computer and Interconnection Architectures" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan
- "Advanced computer architectures", (2.5 Credits) Ph. D. Programme, Computing Systems Engineering, Politecnico di Milano, Milano Leonardo Campus (in collaboration with prof. M. Sami)

Academic Year 2005/2006

- "Architectures for multimedia systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English)
- "Hardware/software co-design methodologies" (10 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus
- "Computer science fundamentals" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus
- "Computer and Interconnection Architectures" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan

Academic Year 2004/2005

- "Architectures for multimedia systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus
- "Hardware/software co-design methodologies" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus
- "Computer science fundamentals" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus
- "Computer and interconnection architectures" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan

Academic Year 2003/2004

- "Architectures for multimedia systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus
- "Computer science fundamentals" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus
- "Computer and interconnection architectures" (12 Credits), Undergraduate Programme, Information and Communication technology, University of Milan

Academic Year 2002/2003

- "Computer Architectures" (10 Credits), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus
- "Computer science fundamentals" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus
- "Computer and Interconnection Architectures" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan

Academic Year 2001/2002

- "Computer Architectures" (10 Credits), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus
- "Computer and Interconnection Architectures" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan
- "Computer Architectures I" (Labs for prof. N. Scarabottolo), Undergraduate Programme, Computer Science, University of Milan, Crema Campus

Academic Year 2000/2001

- "Computer Architectures I" (Labs for prof. N. Scarabottolo), Undergraduate Programme, Computer Science, University of Milan, Crema Campus
- "Computer and interconnection architectures / part II" (6 Credits), Undergraduate Programme, Computer Science, University of Milan
- "Laboratory of operating systems / part I" (6 Credits), Undergraduate Programme, Computer Science, University of Milan
- "Advanced computer architectures", Ph. D. Programme, Computer Science, Department of Computer Science, University of Milan
- "Computer Architectures" (Labs for prof. M. Sami), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus

Academic Year 1999/2000

- "Laboratory of Computer Architectures I" (6 Credits), Undergraduate Programme, Computer Science, University of Milan, Crema Campus
- "Computer Architectures" (Labs for prof. M. Sami), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus
- "Computer Architectures" (Labs for prof. R. Stefanelli), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus

Academic Year 1998/99

- "Electronic Design Automation" (Labs for prof. P. Gubian), Master of Science, Electronics Engineering, University of Brescia
- "Computer Architectures" (Labs for prof. M. Sami), Master of Science, Electronics and

Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus

- "Computer Architectures" (Labs for prof. R. Stefanelli), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus

Academic Year 1997/98

- "Electronic Design Automation" (Labs for prof. P. Gubian), Master of Science, Electronics Engineering, University of Brescia
- "Computer Systems" (Labs for prof. G. Berini), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus

Academic Year 1996/1997

- "Electronic Design Automation" (Labs for prof. P. Gubian), Master of Science, Electronics Engineering, University of Brescia

6.2. OTHER TEACHING ACTIVITIES

- Seminars in the course: "*Design of VLSI Circuits*", Master in Information Technology, CEFRIEL, Milan, A. Y. 1997/98, A. Y. 1998/99, A. Y. 1999/2000 e A. Y. 2000/2001.
- Seminars in the course: "*Computer Architectures*", per la Scuola Interuniversitaria Lombarda di Specializzazione per l'Insegnamento Secondario – Milano Session (SILSIS-MI), Physics – Computer Science – Mathematics (Ref. prof. N. Scarabottolo). A. Y. 1999/2000 e A.Y. 2000/2001.
- Tutorial: "*HD02 – Architectures of VLSI systems*" held at Siemens Mobile Communications, Cinisello Balsamo (MI), 8-9 Sept. 2003 (in collaboration with prof. D. Sciuto, Politecnico di Milano).
- Tutorial: "Introduction to Multiprocessors" held at STMicroelectronics, Agrate B. (Italy), 18/4/2000.
- Tutorial: "Advanced Computer Architectures" held at Alenia Spazio - LABEN, Milan, 25-26 October 2002.

6.3. ACADEMIC RESPONSIBILITIES

- Thesis Committee Member for several undergraduate students and master students in Computer Science at University of Milano, 2000-2002.
- Committee Member, Committee on Undergraduate Studies in Computer Engineering, Politecnico di Milano, Como Campus, 2002-Present.
- Chair, Committee on Undergraduate Studies Approval in Computer Engineering, Politecnico di Milano, Como Campus, 2005-Present.
- Committee Member, Committee on Graduate Admissions in Computer Engineering, Politecnico di Milano, Como Campus, 2002-Present.
- Thesis Committee Member for several undergraduate students and master students in Computer Engineering at Politecnico di Milano, 2002-Present.
- Committee Member, Committee for the comparative evaluation to evaluate the candidates for one position as Assistant Professor (MIUR Researcher) in Computer Engineering, University of Catania, 2007-2008.

6.4. RESEARCH ADVISING

6.4.1. Doctoral Students Supervision

1. **Vittorio Zaccaria, Ph. D.**, currently Assistant Professor at Dipartimento di Elettronica e Informazione, Politecnico di Milano, System Architectures Group. First employment: R&D Engineer at STMicroelectronics in Agrate B. (I) and Manno (CH). Ph.D. Thesis on: "Power exploration methodologies for VLIW-based systems", XIV Ph.D. cycle at Politecnico di Milano, Ph. D. defense: February 2002, Advisor: prof. M. Sami. Co-Advisors: prof. D. Sciuto, Dr. C. Silvano.
2. **Gianluca Palermo, Ph.D.**, currently Assistant Professor at Dipartimento di Elettronica e Informazione, Politecnico di Milano, System Architectures Group. First employment: Post-Doc at Dipartimento di Elettronica e Informazione, Politecnico di Milano. Ph.D. Thesis on: "Design Methodologies for Embedded Architectures based on Network on-Chip", XVIII Ph.D. cycle at Politecnico di Milano, Ph. D. defense: February 2006, Advisor: prof. C. Silvano.
3. **Giovanni Beltrame, Ph.D.**, currently Assistant Professor at École Polytechnique de Montréal. First employment: Microelectronics Engineer at European Space Agency (NL). XVIII Ph.D.

- cycle at Politecnico di Milano, Ph.D. Thesis on “Modeling, Simulating, Analysis and Optimization of Multi-Processor System-on-Chip Platforms”, Ph. D. defense: February 2006, Advisor: prof. D. Sciuto. Co-Advisor: prof. C. Silvano.
4. **Matteo Monchiero Ph.D.**, currently Senior Research Scientist, Intel Labs at Hillsboro (OR, US). First employment: Post Doctoral Research Associate at HP Labs in Palo Alto, CA, Exascale Computing Lab., Ph.D. Thesis on: “Power/performance analysis and optimization of multicore architectures”, XIX Ph.D cycle at Politecnico di Milano, Ph. D. defense: February 2007, Advisor: prof. C. Silvano.
 5. **Oreste Villa, Ph.D.**, currently (and first employment): Research Scientist at the High Performance Computing Group at Pacific Northwest National Laboratory , Richland, WA (USA), Ph.D. Thesis: “Designing and Programming Multi-core Architectures”, XX PhD cycle at Politecnico di Milano, Ph. D. defense: February 2008, Advisor: prof. C. Silvano.
 6. **Giovanni Mariani, Ph. D.**, currently (and first employment): Post-Doc at ALaRI, the Advanced Learning and Research Institute, part of the Faculty of Informatics of the University of Lugano (Switzerland), Ph.D. Thesis: "A Design Space Exploration Methodology Supporting Run-time Resource Management for Multi-Core Architectures", Ph. D. at University of Lugano, Ph. D. defense: March, 2011, Advisor: prof. M. Sami, Co-Advisor: prof. C. Silvano
 7. **Leandro Fiorin**, currently **Ph.D. student** at ALaRI, the Advanced Learning and Research Institute, part of the Faculty of Informatics of the University of Lugano (Switzerland), Ph.D. Thesis: "High level services for Networks-on-Chip", PhD Defense: to be done by March 2012, Advisor: prof. M. Sami, Co-Advisor: prof. C. Silvano.
 8. **Marco Ceriani**, currently **Ph. D. student**, Dipartimento di Elettronica e Informazione, Politecnico di Milano. Co-Advisors: prof. G.Palermo, prof. C.Silvano.
 9. **Edoardo Paone**, currently **Ph. D. student**, Dipartimento di Elettronica e Informazione, Politecnico di Milano.

6.4.2. Undergraduated and Master Students Supervision

1. I was advisors of several Master students in Information Technology at Cefriel Research and Training Center di Milano, EDA (Electronic Design Automation) Group, 1993-1999.
2. I was co-advisors of several Master students in Electrical Engineering at Università degli Studi di Brescia, 1996-1999.
3. I was advisor of several undergraduate and Master students in Computer Science at Università degli Studi di Milano, 2000-2002.
4. I was advisor of about **60** undergraduate students and Master students in Computer Engineering, Electrical Engineering, and Communication Engineering at Politecnico di Milano, 2002-Present.

6.5. PHD EXTERNAL EXAMINER

1. In May 2009, I have been invited as Opponent Member of the Doctoral Examination Committee, Board of the Doctorates, Delft University of Technology (NL) for the Ph.D. defense of the candidate Carlo Galuzzi discussing a thesis titled: "Automatically fused instructions".
2. In February 2011, I have been invited as Opponent Member of the Doctoral Examination Committee, Board of the Doctorates, Delft University of Technology (NL) for the Ph.D. defense of the candidate Kamana Sigdel discussing a thesis titled: "System-level Design Space Exploration of Reconfigurable Architectures".
3. In June 2011, I have been invited as Opponent Member of the Doctoral Examination Committee, Technical University of Catalonia (Spain) for the Ph.D. defense of the candidate Friman Sánchez Castaño discussing a thesis titled: "Exploiting Multiple Levels of Parallelism in Bioinformatics Applications", Advisors: Dr. Alex Ramírez and Dr. Mateo Valero.
4. More recently, in April 2011, I have been invited as Opponent member of the Doctoral Examination Committee, University of Verona, for the Ph. D. defense of the candidate Francesco Stefanni discussing a thesis titled: “A design and verification methodology for networked embedded systems” April 2011. Advisor: prof. Franco Fummi.

6.6. RESEARCH STAFF

1. **Vittorio Zaccaria, Ph. D.**, currently **Assistant Professor** at Dipartimento di Elettronica e Informazione, Politecnico di Milano, System Architectures Group. His current research focuses on design space exploration and parallel programming paradigms and architectures.
2. **Gianluca Palermo, Ph.D.**, currently **Assistant Professor** at Dipartimento di Elettronica e Informazione, Politecnico di Milano, System Architectures Group. His current research focuses

- on design space exploration and Network-on-chip for many-core architectures.
3. **Giovanni Agosta, Ph. D.**, currently **Assistant Professor** at Dipartimento di Elettronica e Informazione, Politecnico di Milano. Formal Languages and Compilers Group. His current research focuses on dynamic compilation for ILP architectures. The main research advisor is professor Stefano Crespi Reghizzi, Politecnico di Milano.
 4. **Sotirios Xydis**, Ph. D. from Technical University of Athens, currently **Post-Doc** at Dipartimento di Elettronica e Informazione, Politecnico di Milano. System Architectures Group. His current research focuses on design space exploration, high level synthesis and programmable architectures.
 5. **Iyad Al Khatib, Ph.D.** from Royal Institute of Technology, Stockholm, Sweden, currently Post-Doc at Dipartimento di Elettronica e Informazione, Politecnico di Milano. System Architectures Group. His current research focuses on design space exploration for multi/many core architectures and pervasive systems for healthcare applications.

6.7. VISITORS

1. **Arpad Gellért, Ph. D., Assistant Professor**, “Lucian Blaga” University of Sibiu, Romania, **Visiting Researcher**, Spring 2009.
2. **Caroline Concatto**, Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 15-01-10 to 15-04-10, FP7 HiPEAC NoE Collaboration Grant.
3. **Debora Matos**, Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 02-02-11 al 02-05-11, FP7 HiPEAC NoE Collaboration Grant.
4. **Anelise Kologeski**, Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 02-02-11 al 02-05-11, FP7 HiPEAC NoE Collaboration Grant.

7. LIST OF PATENTS AND AWARDS

7.1. PATENTS

	Publication number	Publication date	Inventor(s)	Applicant(s)	Application number and date
P1-EU	Integrated CMOS static RAM.				
	EP0578900 (A1)	19/01/1994	SADA GIANCARLO [IT] SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	EP19920830383 - 16/07/1992
	EU Patent Granted EP0578900 (B1)	05/11/1997			
P1-DE	Integrierter CMOS-statischer RAM.				
	DE Patent Granted DE69223046 (T2)	26/02/1998	SADA GIANCARLO [IT] SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	DE19926023046T -16/07/1992
P2-US	Digital information error correcting apparatus for single error correcting (SEC), double error detecting (DED), single byte error detecting (SBED), and odd numbered single byte error correcting (OSBEC)				
	US Patent Granted US5535227 (A)	09/07/1996	SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	US19940248140 - 23/05/1994
P2-EU	Digital information error correcting apparatus for correcting single errors (SEC), detecting double errors (DED) and single byte multiple errors (SBD), and the correction of an odd number of single byte errors (ODD SBC).				
	EP0629051 (A1)	14/12/1994	SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	EP19930830254 10/06/1993
	EU Patent Granted EP0629051 (B1)	01/04/1998			
P2-DE	Digital information error correcting apparatus for correcting single errors (SEC), detecting double errors (DED) and single byte multiple errors (SBD), and the correction of an odd number of single byte errors (ODD SBC).				
	DE Patent Granted DE69317766 (T2)	30/07/1998	SILVANO CRISTINA [IT]	BULL HN INFORMATION SYSTEMS [IT]	DE19936017766T - 10/06/1993
P3-US	Encoder/decoder architecture and related processing system				
	US2002019896 (A1)	14/02/2002	FORNACIARI WILLIAM [IT] SCIUTO DONATELLA [IT] SILVANO CRISTINA [IT] ZAFALON ROBERTO [IT] PAU DANILLO [IT]	ST MICRO-ELECTRONICS SRL [IT]	US20010843533 - 25/04/2001
P3-EU	Encoder architecture for parallel busses				
	EP1150467 (A1)	31/10/2001	FORNACIARI WILLIAM [IT] SCIUTO DONATELLA [IT] SILVANO CRISTINA [IT] ZAFALON ROBERTO [IT] PAU DANILLO [IT]	ST MICRO-ELECTRONICS SRL [IT]	EP20000830322 28/04/2000

P4-US Processor architecture					
US2002124155 (A1)	05/09/2002	SAMI MARIAGIOVANNA [IT]	ST MICRO- ELECTRONICS SRL [IT]	US20010976241 11/10/2001	
		SCIUTO DONATELLA [IT]			
		SILVANO CRISTINA [IT]			
		ZACCARIA VITTORIO [IT]			
		PAU DANILO [IT]			
		ZAFALON ROBERTO [IT]			
US Patent Granted US6889317 (B2)	03/05/2005				
P4-EU Processor architecture with variable-stage pipeline					
EP1199629 (A1)	24/04/2002	SAMI MARIAGIOVANNA [IT]	ST MICRO- ELECTRONICS SRL [IT]	EP20000830673 - 17/10/2000	
		SCIUTO DONATELLA [IT]			
		SILVANO CRISTINA [IT]			
		ZACCARIA VITTORIO [IT]			
		PAU DANILO [IT]			
		ZAFALON ROBERTO [IT]			
P5-US PROGRAMMABLE DATA PROTECTION DEVICE, SECURE PROGRAMMING MANAGER SYSTEM AND PROCESS FOR CONTROLLING ACCESS TO AN INTERCONNECT NETWORK FOR AN INTEGRATED CIRCUIT					
US2009089861 (A1)	02/04/2009	CATALANO VALERIO [FR]	ST MICRO- ELECTRONICS GRENOBLE SA [FR]	US20080207131 - 09/09/2008	
		COPPOLA MARCELLO [FR]			
		LOCATELLI RICCARDO [FR]			
		SILVANO CRISTINA [IT]			
		PALERMO GIANLUCA [IT]			
		FIORIN LEANDRO [CH]			
P5-EU Programmable data protection device, secure programming manager system and process for controlling access to an interconnect network for an integrated circuit.					
EP2043324 (A1)	01/04/2009	CATALANO VALERIO [FR]	ST MICRO- ELECTRONICS GRENOBLE SA [FR]	EP20070301411 - 28/09/2007	
		COPPOLA MARCELLO [FR]			
		LOCATELLI RICCARDO [FR]			
		SILVANO CRISTINA [IT]			
		PALERMO GIANLUCA [IT]			
		FIORIN LEANDRO [CH]			

7.2. AWARDS

- **Bull Technical Award 1991** for my contribution to the project: *“Integrated CAD framework for complex ASIC design”*. The award has been motivated by my contribution to the solution to relevant technical problems demonstrating high professional competences, originality approach and constant personal commitment
- **Best Paper Award SAC 2008**, Applications Theme, 23rd Annual ACM Symposium on Applied Computing, given to the paper: M. Sykora, G. Agosta e C. Silvano *“Dynamic Configuration of Application Specific Implicit Instructions for Embedded Pipelined Processors”*, Fortaleza, Brazil, 16-20 March, 2008.

8. LIST OF PUBLICATIONS

I have co-authored **22** top-ranked journal publications (including **12** IEEE/ACM Transactions) and **13** book chapters. I am co-author of **66** scientific publications on peer-reviewed international conferences (collecting one Best Paper Award and one of the most influential papers published in the Proceedings of DATE Conference in the decade 1998-2008). I am co-author of the book: "Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems", published by Kluwer Academic Publisher (2003). I am co-editor of the books: "Low-Power Networks-on-Chip", Springer (2010) and "Multi-objective design space exploration of multiprocessor SoC architectures", Springer (2011). **My Hirsch's h-index is 18; my Egghe's g-index is 36 and total number of citations is 1525.**

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- [J1]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Space", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**. **Accepted for publication, 2011 (Awaiting production)**.
- [J2]. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "A Variability-Aware Robust Design Space Exploration Methodology for CMPs", **ACM Transactions on Embedded Computing Systems**. Vol. 10, Issue 4, August 2011. **Accepted for publication (Awaiting production)**.
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- [J11]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa, "Efficient Synchronization for Embedded on-Chip Multiprocessors", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Vol. 14, No. 10, October 2006, pp. 1049-1062.
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- This work has been selected to be re-published as Chapter 3 of the book: "*Readings in Hardware/Software Co-design*", Edited by G. De Micheli, R. Ernst, and W. Wolf, The Morgan Kaufmann Series in Systems on Silicon, Jun. 2001, ISBN 1-55860-702-1.
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- [B2]. Cristina Silvano; William Fornaciari; Eugenio Villar; (**Editors**), "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures: The MULTICUBE Approach", Springer, 1st Edition, 2011, XVIII, 222, p. 88 illus. Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011.
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This chapter represents a **re-publication** of the paper [C58].
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8.4. ACADEMIC TEXTBOOKS (IN ITALIAN)

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